A Novel Computational Analog Block for Using in Analog Processors

Yasha Karimi, Mir Mohammad Navidi, Adib Abrishmifar, and Sattar Mirzakuchaki

***Abstract*— In this paper, we propose a computational analogue block which can be used to realize functions such as squaring, harmonic mean calculation, and vector summing. As presented block can be programmed to realize mentioned functions, it can be efficiently employed in systems and applications demanding programmable mathematical blocks like analogue processors. The presented block was simulated in 0.18µm CMOS process at ±0.9V supply voltage; Maximum error for all obtained functions compare to ideal one is below 2%. The simulation results were obtained by Hspice and with high detailed transistor library.**

***Index Terms*— Computational analog block, Squaring Circuit, Harmonic Mean Circuit, Vector Summing Circuit.**

I. Introduction

The aims toward shorter design cycles for analog integrated circuits has caused the development of high performance analog circuits which are reconfigurable and are suitable for CAD methodologies [1]. In signal processing, many applications like filtering require tuning and adaption, Hence a programmable circuit is a beneficial means for this purpose. Moreover, programmable circuits such as Field Programmable Analog Arrays (FPAAs) and Analog Signal Processors (ASPs) deal with many types of linear and non-linear applications requiring more than tuning. In these systems the functions are fundamentally evolved from the combination of several subsystems via programmable internal connections [2]. In order to decrease the parasitic effects of connecting lines, to find subsystems or configurable analogue block (CAB) with higher functionality some attempts are performed [3, 4, 5]. When CABs have higher functionality, the internal connection among them can be decreased, consequently parasitic effects of the connecting lines are diminished and higher performance is achieved [2].

For applications which do not require high computational precision, current-mode analog signal processing (ASP) suggests several advantages over digital signal processing techniques in terms of energy efficiency and speed [6, 7]. By exploiting the computational primitives inherences in the device physics, complicated mathematical functions can be implemented in analog, using significantly lower number of transistors compared to their digital counterparts [8]. The most popular approach for synthesizing current mode analog computational circuits is based on the translinear principle which elicits the exponential current-to-voltage relationship observed in bipolar transistors [9] and metal oxide-semiconductor (MOS) transistors biased in weak-inversion mode [10]. In [11], the translinear principle has also been extended towards synthesizing current-mode circuits using MOS transistors biased in strong-inversion mode. This paper propose a novel configurable analogue block which provides functions like squaring, harmonic mean calculation, and vector summing by its port configurations. Regarding to its low error, this block could be used in analog processors.

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II. Concepts of MTL Circuits

Generally, the MOS Translinear (MTL) equation is concluded for MOS transistors biased in strong inversion mode. The obligatory necessity for MTL circuits is a loop of MOS transistors whose gate-source voltages are connected in series, with equal numbers of transistors being clockwise and counter-clockwise as depicted in Fig. 1. The current sources shown are bias or signal currents and all transistors in this figure are biased to operate in saturation mode**.** Current distribution could be defined by drain nodes connected to the loop or other nodes of the circuit. From Kirchhoff's voltage law, it follows that

$$\sum_{cw} V_{gs} = \sum_{ccw} V_{gs} \qquad (1)$$

Where the subscript cw and ccw represent the transistors connected clockwise and counterclockwise in the loop, respectively.

If we apply the square-law model for an ideal saturated MOS transistor, assuming well-matched threshold voltages (monolithic construction and uniform temperature) and neglecting body effect allows threshold voltages to be dropped. Also the parameters µ and C_{ox} will then be common and thus could be canceled, we have [12]:

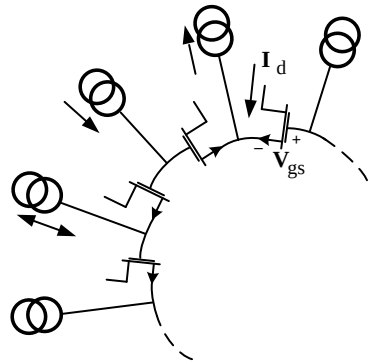

Fig. 1. Conception of MOS translinear Loop [12].

$$\sum_{cw}\frac{\sqrt{I_d}}{W/L}=\sum_{ccw}\frac{\sqrt{I_d}}{W/L} \tag{2}$$

Where W/L ratio is determined by designer.

Equation 2 is a simple algebraic relation between the MOS transistor currents and shows a declaration of the MTL circuit principle and it is insensitive to temperature and processing.
The body-effect is the influence of a source-to-substrate bias on the characteristics of an MOS transistor. The effect is most noticeable as a change in the threshold voltage V_{th}. The influence of body effect can be significantly reduced if an up-down topology is used as indicated in Fig.2. In such a topology the source of each transistor connected clockwise in the loop is connected to the source of another transistor connected counterclockwise in the loop. In [12], Wiegernik showed the influence of the body effect decreases with increasing the V_{sb} value with an "up-down" topology.

III. Proposed Computational Analog Block

A. Current Squaring

Squaring circuits are widely used in many practical applications such as RMS-to-DC converters in instrumentation and non-linear signal generation used in analog signal processing. Notwithstanding the fact that the analog multipliers can achieve the same function, such circuit topologies tend to be more complex with the non-saturation-based squaring circuits. Because of the mentioned benefits of up-down topology, in some papers [13, 14] a current squaring circuit is implemented by means of this structure. In [13], the presented current multiplier and squaring circuit shows very good fastness, accuracy, and bandwidth. Its circuit diagram is shown in Fig.3. In [13] W/L ratios of all transistors are the same; By using Eq. 2 and straight computation and employing the results of translinear loop for MOS transistors biased in strong inversion mode, the relationship between input and output currents will be:

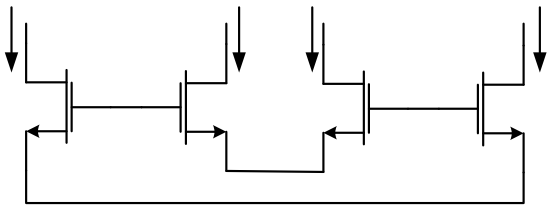

Fig. 2. MOS translinear loop with up-down topology [12].

$$I_{out}=2I_B+\frac{I_{in}^2}{8I_B} \tag{3}$$

And the input current range is given by Eq.4:

$$-4I_B\le I_{in}\le 4I_B \tag{4}$$

In this paper, by modifying the W/L ratios, and by choosing M1 and M3 four times larger than M2 and M4, Eq.3 will be changed to:

$$I_{out}=\frac{I_B}{2}+\frac{I_{in}^2}{2I_B} \tag{5}$$

And the input current will be limited by:

$$-I_B\le I_{in}\le I_B \tag{6}$$

By means of Eq.2 other circuits like vector summing circuit and harmonic mean circuit can be obtained by changing the input and output current ports. In order to use Fig. 3 circuit as computational analog block, we modify its W/L ratio and apply a novel configuration which will be discussed in next sections.

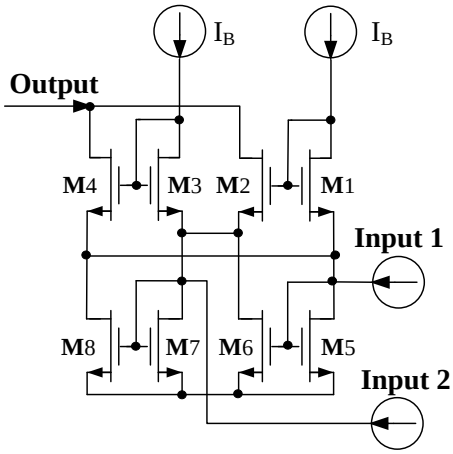

Fig. 3. MOS translinear loop with up-down topology [13].

B. Proposed Harmonic Mean Circuit

Harmonic mean is one of the important mathematic equations which were recently used in edge detection in image processing [15]. In Fig. 3, if we assume both bias currents (I_B) are equal to I_X+I_Y and Input1 and Input2 are equal to I_X and I_Y respectively and I_X+I_Y is summed with output current, Then we will have harmonic mean of input currents at output current. Fig. 4 shows the harmonic mean calculating configuration extracted from Fig. 1 and Eq. 7 shows the relationship between output and inputs. In this configuration $I_X+I_Y > 0$ should be considered.

$$-I_{out}+I_X+I_Y=\frac{I_x+I_Y}{2}+\frac{\left(I_x-I_Y\right)^2}{2\left(I_X+I_Y\right)}$$

$$\rightarrow -I_{out}+I_x+I_Y=\frac{2I_X^2+2I_Y^2}{2\left(I_X+I_Y\right)}$$

$$\rightarrow I_{out}=\frac{I_X^2+I_Y^2+2I_xI_Y-I_X^2-I_Y^2}{\left(I_X+I_Y\right)}$$

$$I_{out}=\frac{2I_xI_Y}{\left(I_X+I_Y\right)} \qquad (7)$$

C. Proposed Vector Summing circuit

The vector summation is a nonlinear signal processing function finding application in a wide variety of instrumentation, communication, and control systems. Some vector summation circuits have been published previously in the literature [16-18] with inputs in either voltage or current mode. In this article by considering IOUT+IY for IB and IX for input1 current and zero value for input2 current in Eq.5, we will have Eq. 8 which shows that IOUT is the vector sum of IX and IY. Fig. 5. shows the circuit structure of vector summing circuit which exploits MOS translinear loop with up-down topology. Consider that IY should be greater than zero in this structure.

$$I_{OUT}=\frac{I_Y+I_{OUT}}{2}+\frac{\left(I_x\right)^2}{2\left(I_{OUT}+I_Y\right)}$$

$$\rightarrow \frac{\left(I_{OUT}-I_Y\right)}{2}=\frac{\left(I_x\right)^2}{2\left(I_{OUT}+I_Y\right)}$$

$$I_{OUT}^2-I_Y^2=I_X^2$$

$$I_{Out}=\sqrt{I_X^2+I_Y^2} \qquad (8)$$

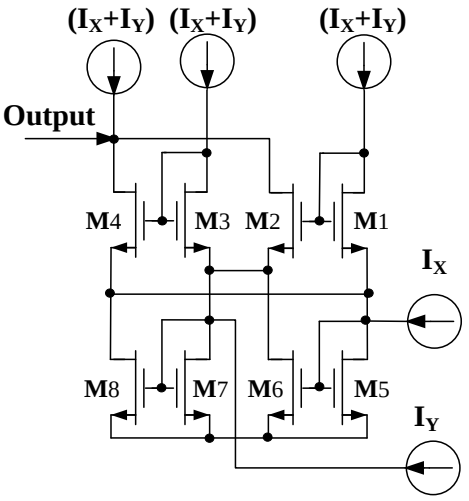

Fig. 4. Proposed configuration for harmonic mean calculation.

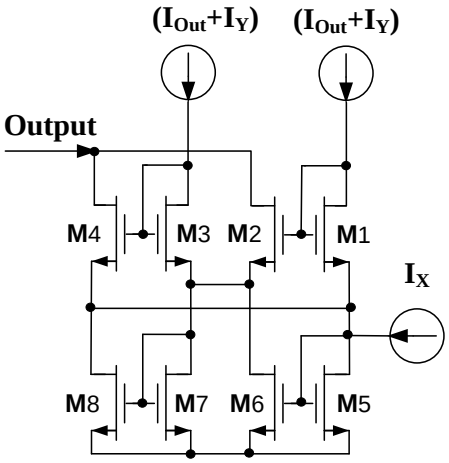

Fig. 5. Proposed configuration for vector summing.

D. Proposed Configuration for presented CAB

To generate all above functions (current squaring, harmonic mean, and vector summing) in an analog processor or FPAA, a programmable configuration is needed. In other words, the designer should be able to realize all mentioned functions by programming single block.

In Fig. 6 (a) symbol of fig.3 is demonstrated. In this symbol, we show input 1, input 2, I_B, and output current with I_1, I_2, I_B (considering same current for both bias input), and I_O, respectively. In Fig. 6 (b), a possible configuration using a squaring block and three programmable current mirrors is presented. The numbers in programmable current mirror in Fig. 6 is demonstrated in Fig. 7. By programming the current mirror, all three functions are achievable.

There are many structures which can be used for programmable current mirrors. The current copier can also be used instead of current mirrors. In this paper, we use a famous current mirror, low voltage low power current mirror [19], which has good accuracy and bandwidth. This current mirror with programming switches is shown in Fig. 7.

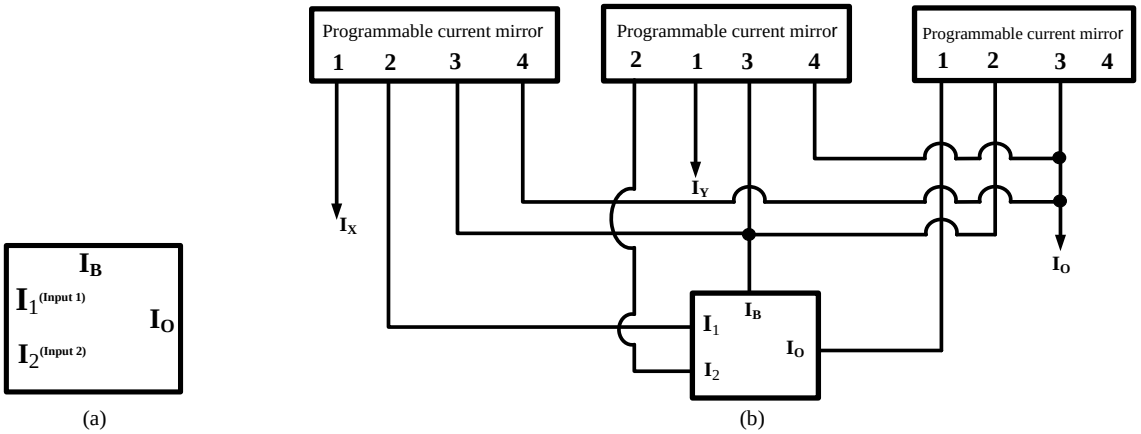

Fig. 6. (a) Symbol of Proposed Block for circuit in Fig. 3, (b) configuration for presented Computational Analogue block.

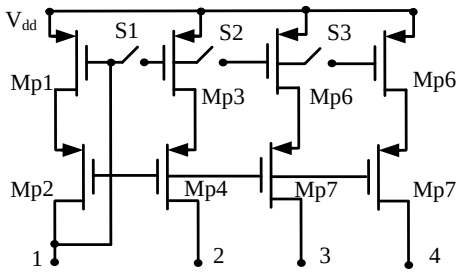

Fig. 7. Presented programmable current mirror used in Fig.6 based on current mirror in [19].

TABLE I
TRANSISTORS ASPECTS OF FIG.3 AND FIG.7 CIRCUITS

Transistors	(W/L)(μm)
M1, M3	8.01/1
M2, M4	2.16/1
M5-M8	7.55/1.88
Mp1-Mp7	9.9/0.18

IV. SIMULATION

A proposed configurable analogue block was designed in 0.18μm CMOS technology with ±0.9V supply voltage, and the simulated results were obtained by HSPICE simulator. The dimension values of all transistors are demonstrated in Table.1 and the simulation results are shown in Fig. 8-13.

In Fig. 8 (a) and (b), the overall and partial DC characteristic of squaring circuit is shown. The dashed line is an ideal representation of Eq. 5 and solid line shows the simulation results for squarring circuit. When input current is sweeped between -50 μA to +50 μA, and the bias currents are fixed at 100 μA, the output error of squared current compared to ideal squared output is less than 0.51%. This error will be 1% at much when input current is varying between -100 to +100 μA.

Fig.9 shows the transient simulation of output current when the input current frequency is 50MHz and its magnitude is 40 μA. Total Harmonic Disortion (THD) of the output squared current is 2.3%.

The tempreature effect on squaring circuit is investigated by assuming different input 1 currents and a constant input 2 current and fixed bias currents (I_{B1} and I_{B2}) both at 100μA. By sweeping the temperature from -40 to 100 C° and considering differetnt input 1 currents, ouput variation will be lower than 1.8% as shown in Fig. 10.

Fig. 11 displays the frequency response of the squaring block. The 3db cut-off frequency of this circuit is about 344MHz.

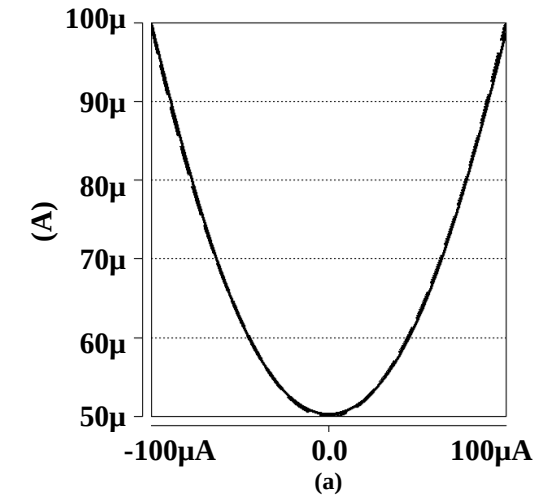

Fig. 8. (a) The overall DC characteristic of current squaring (b) Closed view at the DC characteristic of current squaring.

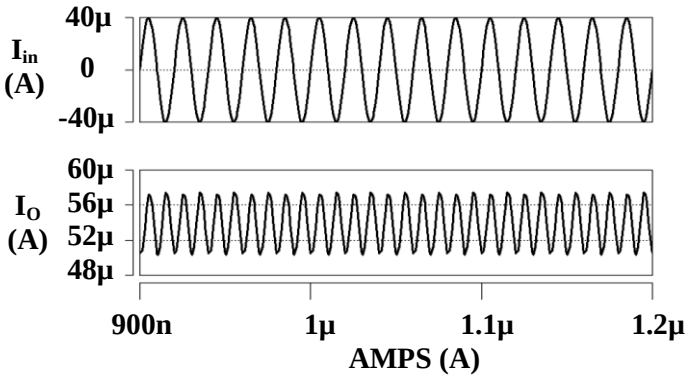

Fig. 9. Transient analysis of current squaring circuit.

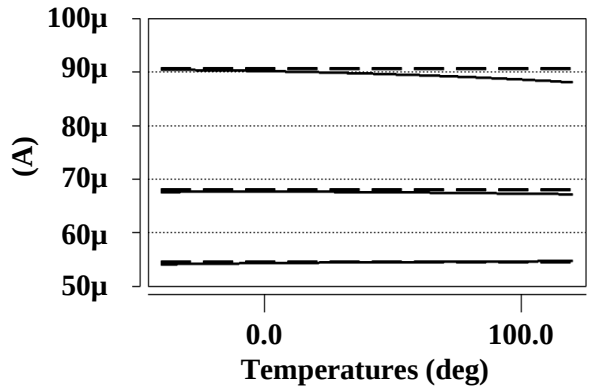

Fig. 10. Output of current squaring along with temperature variations.

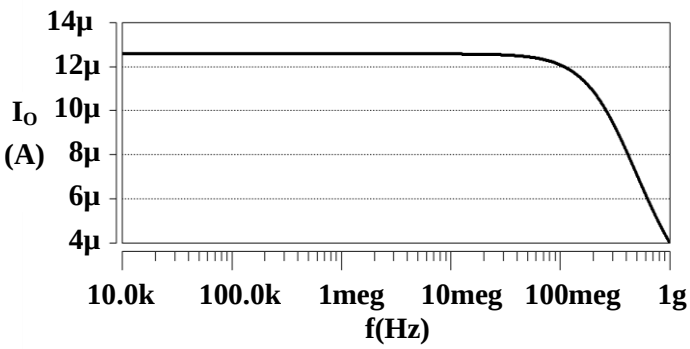

Fig. 11. Frequency response of current squaring circuit.

Fig. 12 shows the DC characteristic of harmonic mean calcualting circuits; In this figure dashed line is the representation of Eq. 7. Regarding to Fig. 12, when I_X is varying from 0 to 60µA and I_Y is constant at 10µA, the output error of the circuit compared to ideal output is less than 2%.

In Fig. 13, the output result for vector summing circuit is depicted. Like previous figures, Dashed line is an ideal schematic of Eq. 8. When input is varying from 1µA to 73.6µA and I_Y is constant at 10µA, the output error compared to ideal case is less than 1.9% .

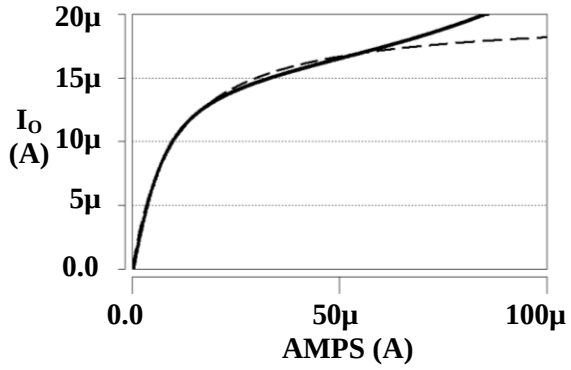

Fig. 12. The DC characteristic of harmonic mean circuit.

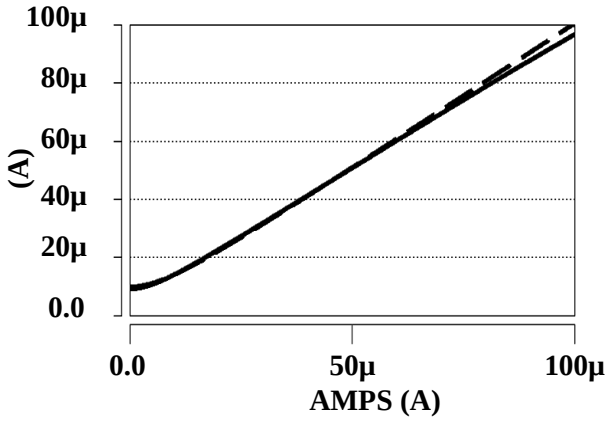

Fig. 13. The DC characteristic of vector summing circuit.

V. Conclusion

In this paper, we proposed a modified current squaring for computational analogue block. By means of this block functions such as current squaring, harmonic mean calculation, and vector summing can be realized just by programming one of the presented CAB. It is also possible to obtain more functions by using several blocks of the proposed CAB or by applying another block like Opamps or OTAs with presented CAB.

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