Design and FPGA Implementation of Frames Detector for SC-FDE/OFDM Millimetre Wave IEEE802.15.3c WPAN

Khaled Sobaihi, Akram Hammoudeh, David Scammell

***Abstract*—The millimetre-wave frequency range 57-64 GHz has been already standardised by the IEEE 802.15.3c for Wireless Personal Area Network (WPAN). The specified PHY targets multi-Giga bit per second data rate with two modes, Single-Carrier Frequency Domain Equalization (SC-FDE) and Orthogonal Frequency Division Multiplexing (OFDM), both modulation schemes are based on framed data transmission, hence, a frame detection mechanism is required.**

In this paper, a frame detector is designed and implemented on FPGA chip; this frames detector targets both modes SC-FDE and OFDM defined by the IEEE 802.15.3c millimetre wave standard. The performance of the implemented detector has been evaluated in both transmission modes, bit-error-rate (BER) is shown as function of signal to noise ratio (SNR) in AWGN and multipath radio channels with line-of-sight and non line-of-sight conditions.

***Index Terms*—60GHz, FPGA, Frames Detector, IEEE802.15.3c, Millimetre-Wave, OFDM, SC-FDE.**

I. Introduction

The 60 GHz millimetre wave frequency band (57-66 GHz in Europe) has drawn an increasing interest over recent years to enable multigigabit-per-second wireless transmission for consumer electronics. TG3c Task Group has already released the IEEE 802.15.3c Wireless Personal Area Network (WPAN) standard to provide up to 5 Gb/s data rate for high speed internet, HDTV video stream and wireless data bus for cable replacement. The IEEE802.15.3c Standard proposed two modulation schemes, Single-Carrier with Frequency Domain Equalization (SC-FDE) for low power low cost application, and Orthogonal Frequency Division Multiplexing (OFDM) for bidirectional high-speed wireless communication [1].

Field Programmable Gate Arrays (FPGAs) have become an attractive option to replace Application Specific Integrated Circuit (ASICs) for prototyping and final product release. Nowadays FPGAs are not just a massive array of inter-connectable gates, but contain dedicated DSPs, RAMs and embedded processors to perform arithmetic operations that would be required for third and fourth generation wireless communication systems. Hence, FPGA-based DSP capabilities combined with an expanding array of Intellectual Property (IP) cores and system level development tools, have made the implementation of Software-Defined Radios (SDRs) where physical components are implemented with software functions using FPGAs possible [2], [3], [4].

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II. Golay Sequences Based Preamble

Recently, Golay complementary sequences have been proposed in the third cellular and WLANs standards, for use in the preamble for synchronization and channel estimation. Golay sequences have been widely used to detect a signal immersed in noise. A pair of Golay sequences (a_N, b_N) have an attractive property that the addition of their a-periodic auto-correlation functions equals to zero for all nonzero time shifts, in other words, the sum of their auto-correlations has maximum peak and no side-lobes [5]. Let [a_N, b_N] be the pair of complementary Golay sequences of length equals to $N=2^M$ (M natural number) and [R_a, R_b] the auto-correlation of a_N and b_N respectively, the Golay sequences are defined by the following auto-correlation property:

$$\mathrm{R_{ab}}(i) = R_a(i) + R_b(i) = 2\mathrm{N}\delta(i-N) \quad (1)$$

Where $\delta_{(i)}$ is the Kronecker delta function.

Golay sequences have not only excellent autocorrelation property, but also a low complexity correlator. An efficient matched filter directly related to the sequences {a_N, b_N} is given in Fig. 1. This matched filter performs simultaneously the correlation of the input signal $x_{(k)}$ with the two complementary sequences {a_N, b_N}, the two corresponding outputs produce the two a-periodic correlation functions {R_a, R_b}. Such digital matched filter is called an Efficient Golay Correlator (EGC). For binary Golay sequences of length 2M, the number of multiplications and additions equal to $\log_2$ M and 2×$\log_2$ M respectively, while in straightforward matched filter implementation it would be M and M-1 respectively [5].

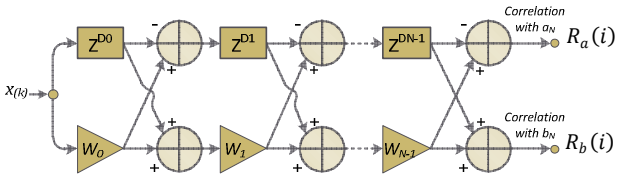

Fig. 1 Efficient Golay Correlator (EGC)

Fig. 2 shows the structure of the preamble proposed by the IEEE 802.15.3c, used for both SC-FDE and OFDM modulation scheme. At the beginning of the frame, the PHY preamble is added to aid the receiver's algorithms related to

automatic gain control, timing and carrier frequency recovery, it consists of synchronization (SYNC) part, for higher robustness it is made of 14 code repetitions of a128 and mainly used for frame detection. The Start Frame Delimiter (SFD) defines the beginning of header frame and header rate, and consists of [a128 -a128 a128 –a128] or [a128 a128 -a128 –a128] for medium and high rate respectively. For channel estimation, the Channel Estimation Sequences (CES) are employed and contain the a256 and b256 Golay complementary sequences. The frame header conveys information about the PHY and MAC (i.e. modulation schemes, coding, and spreading factor). To apply Fourier Transform (FFT), The data is mapped into sub-blocks in both SC-FDE and OFDM which contains data samples or subcarriers respectively [1].

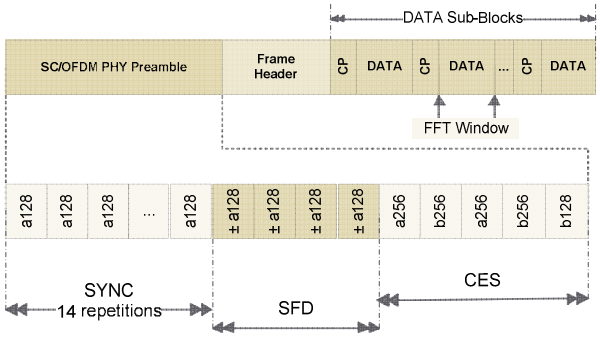

Fig. 2 Frame of the IEEE802.15.3c for the SC-FDE/OFDM Modes

III. FRAMES DETECTOR

Fig. 3 illustrates the block diagram of implemented frame detector, to detect the 'a128' Golay sequences an EGC matched with the respective sequences is used, the normalized EGC's output R_a is then auto-correlated twice with a its shifted copy by 128. The correlation output contains positive and negative peaks that tag the sequences of the SYNC and SFD preambles. Fig. 4 shows the EGC's output and the correlated signal.

To detect the presence of the SYNC and SFD sequences, the correlated signal is compared to a negative threshold; when the negative peaks are present the comparator's output goes high otherwise is low. Emulation results of the miss and false detection probabilities for Signal-to-Noise Ratio of 0dB are shown in Fig. 5. Using a high threshold the detection of the preamble can be missed; whereas, a low threshold leads to false alarms. The optimal value of the threshold is located between the two graphs where miss and false detection are minimum.

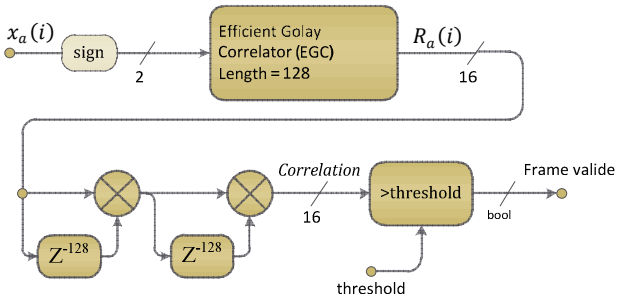

Fig. 3 Block Diagram Schematic of the Frame Detector

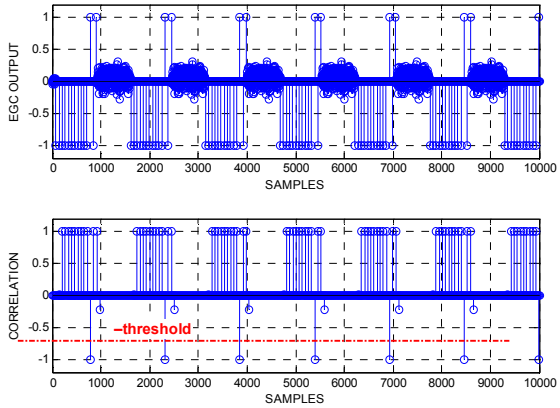

Fig. 4 EGC's Outputs and its Double Correlation

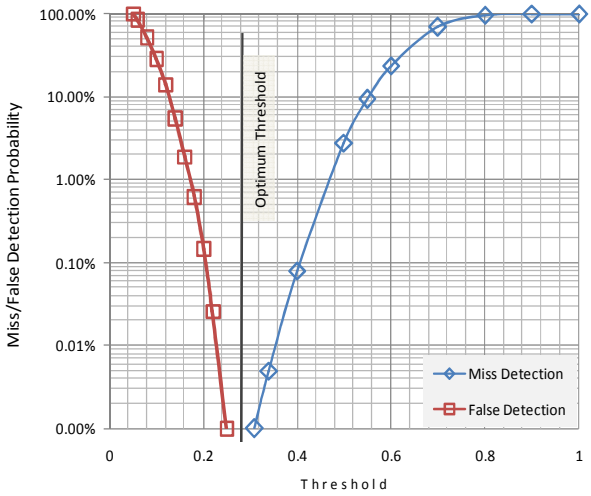

Fig. 5 Probability of Miss and False Detection for SNR = 0 dB

IV. DUAL-MODE SC-FDE/OFDM TRANSCEIVER

To evaluate the performance of the introduced frame detector, a dual-mode SC-FDE/OFDM transceiver has been design and implemented on FPGA. Fig. 6 shows the baseband of the implemented dual mode SC-FDE/OFDM transceiver [6], [7]. In OFDM system the inverse fast Fourier transform (IFFT) transform is placed at the transmitter to map the data symbols into subcarriers. Whereas, in SC-FDE the IFFT is placed at the receiver to transform the equalized spectrum to time domain for demodulation [8].

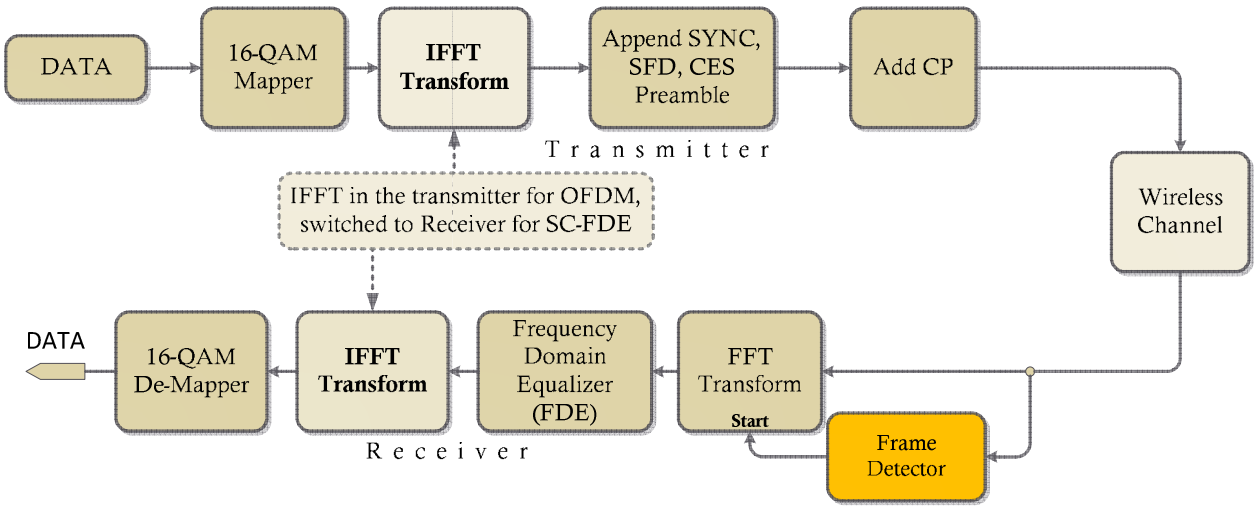

Fig. 6 Dual-Mode SC-FDE/OFDM Transceiver

At the transmitter, data is modulated by using 16-QAM modulation scheme. In OFDM the modulated 16-QAM symbol are mapped into subcarriers with IFFT transform, the preamble of Fig. 2 is built and cyclic prefix (CP) is inserted between data blocks, whereas, in SC-FDE mode the modulated symbols are kept as one carrier, then preamble is appended before the signal being transmitted. At the receiver, and in order to apply FDE equalization on both SC-FDE and OFDM transmission, frame detector described in section III is employed, this detector triggers the Fourier transform FFT of the received signal at the exact start position of channel estimation sequences CES and each data block. After that FFT transform is performed a frequency domain equalization (FDE) is applied to compensate the multipath effect of the radio channels, the equalized symbols are then demodulated with 16-QAM de-mapper to extract the transmitted data. TABLE I shows the parameters of the implemented SC-FDE/OFDM system.

TABLE I
SC-FDE/OFDM SYSTEM PARAMETERS

Parameters	Specification
FFT Size (N)	256
Cyclic Prefix (CP) Length	32
Signal Bandwidth	78MHz
Modulation	16-QAM
Spectrum Efficiency	2.5bit/s/Hz
Maximum Bit-rate	200 Mb/s

V. FPGA IMPLEMENTATION

For the rapid FPGA prototyping of the frame detector the Xilinx System Generator for Matlab Simulink is used. System Generator is a system-level DSP design tool that enables the use of the Mathworks model-based design environment Simulink for FPGA design. Designs are captured in the DSP friendly Simulink modelling environment using a Xilinx specific blockset. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. Fig. 7 shows the design flow performed in System Generator, the design starts by fixed-point simulation and validation using Simulink as the modelling interface with system generator building blocks. Once the design is verified and validated, it is translated into efficient HDL language along with the integration of the Intellectual Property Cores (IP Cores). The design is then synthesized, placed and routed into the FPGA by means of an automatic process [9].

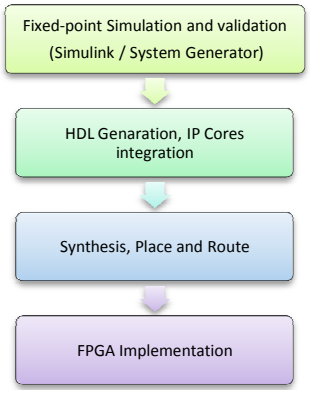

Fig. 7 FPGA Prototyping Design Flow with System Generator

TABLE II shows the FPGA's resources utilization by the frame detector, including the EGC and the correlator with 16 bit data path.

TABLE II
RESOURCES USED ON VIRTEX-4 FPGA

Resources	Resources Used / Available	% of Used Resources
Flip Flops (FFs)	**443** / 30,720	**1 %**
Lookup Tables (LUTs)	**406** / 30,720	**1 %**
Logic Slices	**232** / 15,360	**1 %**
DSP48s (Embedded Multipliers)	**2** / 192	**1 %**

Once the full baseband transceiver design completed, the system generator automatically translates the design into VHDL code, then synthesises, places, and routes the VHDL code to generate FPGA bitstream along with a Simulink library that stores the hardware co-simulation block.

The hardware co-simulation block is then used in Simulink design like other blocks are used. During simulation, the hardware co-simulation block interacts with the FPGA board, automating tasks such as FPGA configuration, data transfers, and clocking. The hardware co-simulation block exchanges data between host PC and FPGA board over the shared memories, where in this case hardware co-simulation interface allows shared memory block and its derivatives (e.g., shared FIFO and shared Registers) to be integrated in the FPGA and mapped transparently to common address spaces on the host PC. Hence, shared memories can help facilitate high-speed data transfers between the host PC and FPGA, and provide a tool for real-time hardware co-simulation. Fig. 8 shows the hardware co-simulation design, a FIFOs memory are employed to exchange data between the host PC and FPGA device or exchange a single value with shared registers.

For this purpose, the 'XtremeDSP' Development Kit-IV is used as development platform that employs the Virtex-4 XC4VSX35-10FF668 FPGA technology from Nallatech. The development Kit uses dual channel, high performance ADCs (14-bits up to 105 MSPS) and DACs (14-bits up to 160 MSPS) [10].

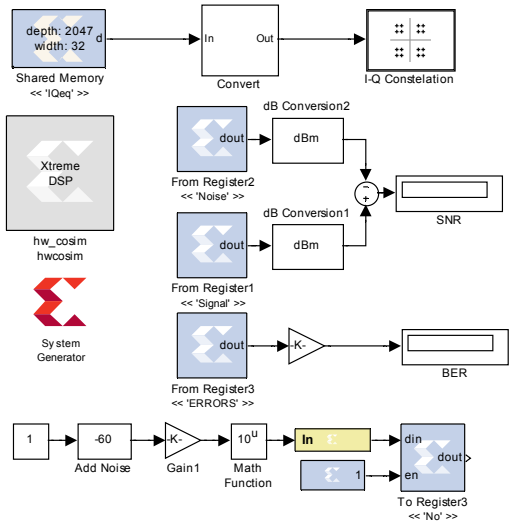

Fig. 8 System Generator Hardware Co-Simulation with Shared Memories

VI. Performance Evaluation of the Detection Performance

The performance of the implemented frame detector has been characterized by the mean of Packet-Error-Rate (PER) versus Signal-to-Noise Ratio (SNR). As shown in Fig. 9, the frames that contains preambles is built and stored in Read Only Memory (ROM) then continuously transmitted, a power adjustable white Gaussian noise is added to the generated signal, in order to emulate an additive white Gaussian noise channel (AWGN). To emulate the effect of multipath channels, the AWGN channel is cascaded with a 60 GHz multipath channel; both emulated channels are implemented on the same FPGA. The multipath channel model is based on T-SV (Two-path Saleh-Valenzuela) model, which has been accepted by the IEEE 802.15.3c channel modelling subcommittee. This model combines a Line-of-Sight (LOS) component using a two-path model with the Non-Line-of-Sight (NLOS) reflective clusters of the Saleh-Valenzuela model [11], [12].

The emulated models reflect the multipath scenarios of residential, desktop and office with line-of-sight (LOS) and non-line-of-sight (NLOS) transmission. Fig. 10 illustrates snapshots of the impulse and frequency responses of some of the used IEEE 802.15.3c multipath channel models. Those are the typical residential CM1.1 LOS and desktop CM4.2 NLOS indoor channels with low and severe multipath dispersions respectively.

To measure PER vs. SNR, a second path is implemented as reference as shown in Fig. 9, packet-error-rate is detected by comparing the two received packets; where the detector works in ideal and real conditions.

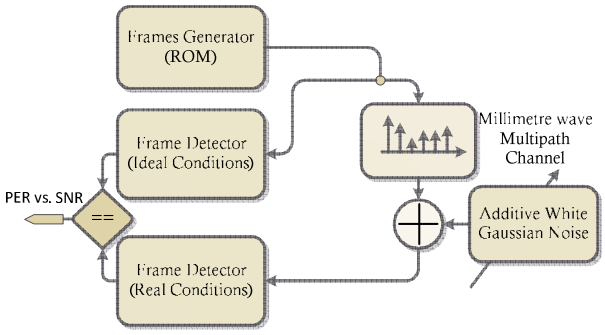

Fig. 9 FPGA Test-bed for the Implemented Frame Detector

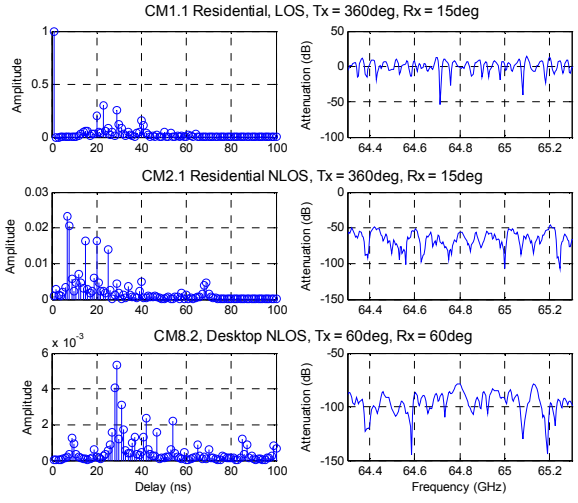

Fig. 10 Impulse and Frequency Response Snapshots of the IEEE 802.15.3c Channel Models

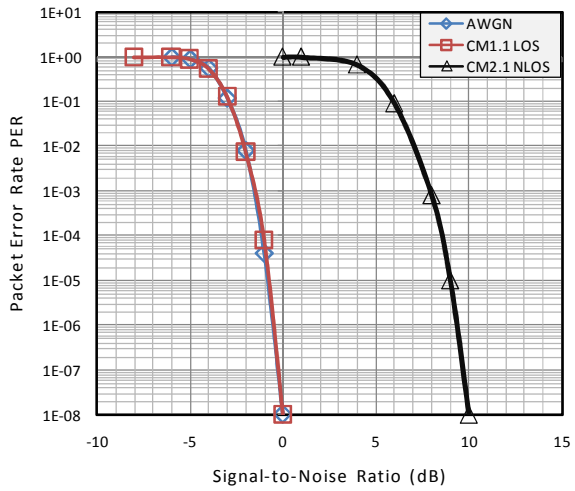

Fig. 11 PER vs. SNR for AWGN, line of sight (LOS) and non line-of-sight (NLOS) Channels

Fig. 11 shows the measurements of the PER vs. SNR over AWGN, and multipath LOS/NLOS channels of a residential environment. The AWGN and LOS channels shows similar results, a very low SNR (less than 0dB) is required to achieve the required 10^{-3} PER, the NLOS channel introduces an important increase of the number lost packets and at least an SNR of 8 dB is required to keep the PER bellow 10^{-3}.

VII. Performance with Dual-Mode SC-FDE/OFDM Transceiver Over Emulated Multipath Channels

Firstly, the performance of the implemented SC-FDE/OFDM transceiver that employs the proposed frame detector has been characterized by measuring bit-error-rate (BER) versus signal-to-noise ratio (SNR) over an additive white Gaussian noise channel (AWGN). As shown in Fig. 12, a power adjustable white Gaussian noise is added to the received signal, in order to emulate the AWGN. The AWGN channel is cascaded with the modelled millimetre wave multipath indoor channels with impulse and frequency responses illustrated in Fig. 10.

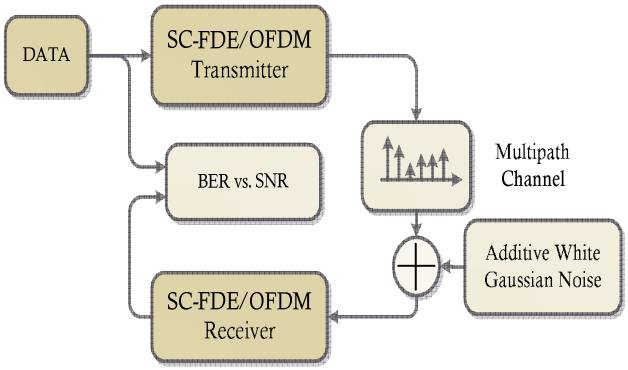

Fig. 12 Test-Bed for the Implemented SC-FDE/OFDM Transceiver

Fig. 13 shows the measurements of the BER vs. estimated SNR conducted over the different multipath and AWGN channels with 16-QAM SC-FDE modulation scheme. Results show that BER results over the CM1.1 and CM8.2 (i.e. channels with moderate multipath and 15° horn antenna at the receiver), matches exactly that of an AWGN channel.

For channels exhibiting more sever selective fading such as residential CM2.1 with NLOS transmission and Omni-directional antenna at the receiver, BER of 10^{-6} is achievable with SNRs of 0.4 dB above those of an AWGN channel.

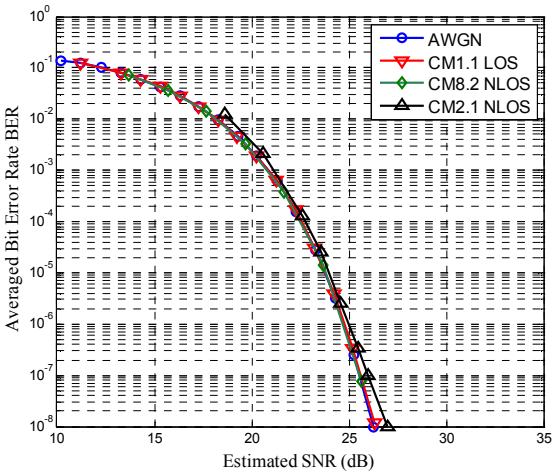

Fig. 13 Measured BER vs. SNR over AWGN and Multipath Channels with SC-FDE Modulation

Fig. 14 shows the measurements of the BER vs. estimated SNR conducted over the different multipath channels with 16-QAM OFDM modulation scheme. Results show that to achieve a BER of 10^{-6}, SNR of 0.5, 1 and 2 dB over that for an AWGN channel is needed for a residential line-of-sight channel (CM1.1), residential non-line-of-sight (CM2.1) and desktop (CM8.2) channels respectively.

TABLE III summarises the results of the SNR required to achieve a BER of 10^{-6} over AWGN and different multipath channels with SC-FDE and OFDM transmission modes.

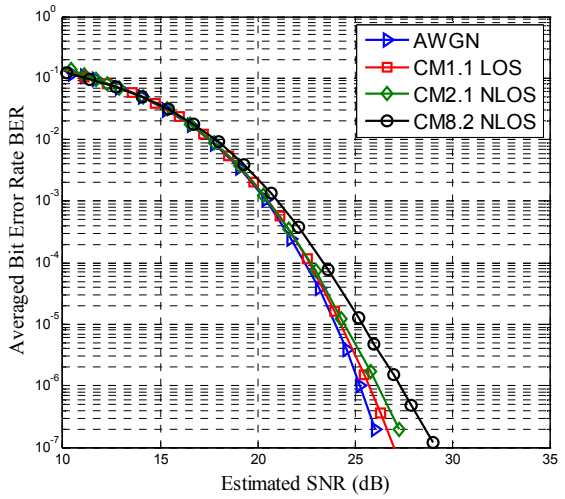

Fig. 14 BER vs. SNR over AWGN and Multipath Channels With OFDM Modulation

TABLE III
SNR REQUIRED FOR SC-FDE/OFDM TO ACHIEVE A BER OF 10^{-6} OVER AWGN AND MULTIPATH CHANNELS

Channels	SNR Required for BER=10^{-6}	
	SC-FDE	OFDM
AWGN	24.6 dB	25.2 dB
Residential line-of-sight (CM1.1)	24.6 dB	25.7 dB
Desktop non-line-of-sight (CM8.2)	24.6 dB	27.2 dB
Residential non-line-of-sight (CM2.1)	25.0 dB	26.2 dB

VIII. CONCLUSION

In this paper, a frame detector for millimetre wave IEEE 802.15.3c standard has been presented, designed and implemented on FPGA. The robustness of the implemented detection mechanism has been evaluated over AWGN and line-of-sight/non-line-of-sight multipath channels with both SC-FDE and OFDM transmission modes. The packet-error-rate versus signal-to-noise ratio measurements has shown that a low signal-to-noise ratio of 1.5 and 8 dB is required over line-of-sight and non-line-of-sight respectively in order to achieve the maximum 10^{-3} PER required by the IEEE 802.15.3c standard.

Furthermore, bit-error-rate (BER) vs. signal-to-noise ratio (SNR) of both SC-FDE and OFDM transmission modes, with 256 points FFT and 16-QAM modulation scheme have been measured. For SC-FDE mode, BER vs. SNR results have shown that BER performance similar to that of AWGN channel for residential LOS and desktop NLOS environments CM1.1 and CM8.2 obtained. However, in a hostile multipath environment, residential with non line-of-sight CM2.1 channel, only 0.4 dB above the AWGN channel is required to achieve 10^{-6} BER. The performance of frame detector with the OFDM transmission mode has shown that a maximum SNR degradation of 2 dB above that of AWGN is required to achieve a BER of 10^{-6} in desktop non line-of-sight environment CM8.2.

The BER vs. SNR results in both SC-FDE and OFDM transmission modes, have shown the robustness of the proposed frame detector in either LOS or NLOS conditions, the FPGA implementation of the proposed detector consumed only 1 % of the available FPGA resources. The amount of the remaining resources are indispensable to implement both transmission modes, SC-FDE and OFDM.

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David Anthony Scammell received BSc in Information Technology and MSc in Electronic Product Engineering from the University of Glamorgan, Wales in 1996 and 1997. He worked in the area of embedded system design before re-joining the University of Glamorgan to pursue a PhD degree on wideband millimetre wave channel modelling and countermeasure techniques. In 2001 he was appointed as a Senior Lecturer in the School of Electronics and specializes in telecommunication, computer programming and embedded design.