A Low Voltage Highly Linear CMOS Down Conversion Mixer

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***Abstract*—In this paper a new low voltage CMOS mixer is proposed which is highly linear. Linearity is provided by adjusting the value of a resistor and sizing the aspect ratio of a PMOS transistor at the RF stage of a well known low voltage CMOS mixer. Simulation results of improved mixer in a 0.18µm CMOS technology illustrate 20 dB increases in IIP3. The mixer can operate at the minimum supply voltage as low as 1 V and the additional components which are used for improving linearity would not increase the power consumption significantly.**

***Index Terms*— CMOS mixer, highly linear, third-order distortion, Volttera series.**

I. Introduction

In recent years, significant growth in wireless communication systems led to the development of low-voltage radio frequency integrated circuits. Receivers can be divided into two parts, RF front-end part and digital part. The former does the transmission and reception of signals and the latter has the duty of signal processing. The RF front-end part needs more power. So, if the power consumption of this part is reduced, the receiver power consumption decreases significantly. Therefore, the low power operation of different blocks in RF front-end is desired [1]. Mixer is one of the several major structural blocks in the RF front-end part which determines the overall linearity of the RF front-end. Then, the investigation of its linearity is very important. In nowadays technology, linearity of receivers due to lower supply voltage is reduced. Harmonic generation, gain compression, inter-modulation, blocking, desensitization and cross-modulation are caused by nonlinearity in the RF front-end [2].

Mixers are composed of two stages: RF stage and switching stage. As linearity in mixers is controlled primarily by the quality of the RF stage, additional ways are reported for extending linearity of this stage. Source degeneration is a commonly used method for linearity improvement. Predistortion, feedback and feedforward are other methods of linearity improvement. In predistortion one, two nonlinearities that are inverses of each other will be summed and then nonlinearity will be removed. But careful matching is needed in this method [3]. Negative feedback computes an estimate of error, inverses it, and adds it back to the input, thereby helping to cancel the error that distortion represents. A feedback system computes the error of a posteriori system, thus its overall close-loop bandwidth must be a small fraction of the inherent bandwidth capabilities of the elements comprising the system.

In the feedforward method, at the same time of processing the signal, estimation of error is done, thereby problems of bandwidth and stability of negative feedback can be solved but the maximum distortion reduction in this method is lower than the negative feedback method [4]. In all these three methods, there is a need for additional circuits which increase active area and power consumption.

Using Multiple Gated Transistors (MGTR) is a novel method for improving linearity in RF stage. In MGTR a second transistor is used in combination with main transistor in RF stage. The bias and size of the secondary transistor is adjusted so that the third-order harmonic distortion can be removed in this combination but the mixture of the second harmonic and fundamental one due to inherent feedback in the circuit, reduces the amount of expected improvement [5].

Some topologies are explained for removing second harmonic distortion and solving this problem. In these topologies, two inductors are used as source degeneration [6], and a voltage source is applied to bulk-to-source of transistors in RF stage [7]. In all these methods, the second distortion harmonic is even eliminated or adjusted to avoid combination with fundamental harmonic and creating third-order distortion.

In this paper, we use the idea of adding a resistor and a PMOS transistor operating in weak inversion into RF stage. In our design we use source termination for output of RF stage. Then parasitic gate-source capacitors have a path of input to output at this stage and they create an option for improving linearity, too. This paper is organized as follows: section II explains the linearity of a common RF stage. The proposed mixer and the method utilized for improving its linearity are explained in section III. Finally, the simulation results and conclusion are presented in sections IV and V, respectively.

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II. LINEARITY OF THE RF STAGE OF A COMMON MIXER

The RF stage has main role in the third-order distortion in mixers. In the RF stage of a common mixer, just a common source transistor is used as an amplifier. Nonlinearity of a common source amplifier in this stage is mostly controlled by nonlinearity of transconductance (g_m) of the employed transistor. For better understanding, Taylor series expansion of a common source amplifier is provided as follows:

$$i_{DS} = I_{dc} + g_m v_{gs} + \frac{g_{m1}}{2!} v_{gs}^2 + \frac{g_{m2}}{3!} v_{gs}^3 + ... \quad (1)$$

Where g_{m1} and g_{m2} are first and second order derivative of g_m with respect to gate-source voltage (V_{gs}), respectively.

As it is realized from (1), g_{m2} has an important role in third-order distortion. There is a very small range about the threshold voltage of transistors which g_{m2} stays very close to zero. But, it is difficult to adjust bias point of transistor in this short range and furthermore, in this range, the gain, noise, and power performance of transistors in RF stage degrades [5]. Then, some additional components must be used in this stage for removing the coefficient of third-order distortion. In the next section, a technique is introduced for improving linearity of this stage.

III. THE PROPOSED MIXER

A. Multiplier Based Mixer Circuits

Although Gilbert cell multiplier is the commonly used structure which is employed as down-conversion mixer in many cases, but it cannot act as a low voltage structure for its stacked elements of RF transistors, switching transistors, current sources and loads. Several methods have been introduced to make its low voltage operation possible but further reduction of voltage is still challenging.

Shown in Fig. 1, a low voltage multiplier is used as a main circuit in our proposed mixer. In this structure, a current signal proportion to radio frequency signal is injected in the common node a(b) and is controlled by another signal. Then the modulated signal obtained at the output contains the multiplication of the two differential inputs. As can be seen in Fig. 1, this structure is composed of two voltage to current converters which are connected in parallel to a pair of voltage follower.

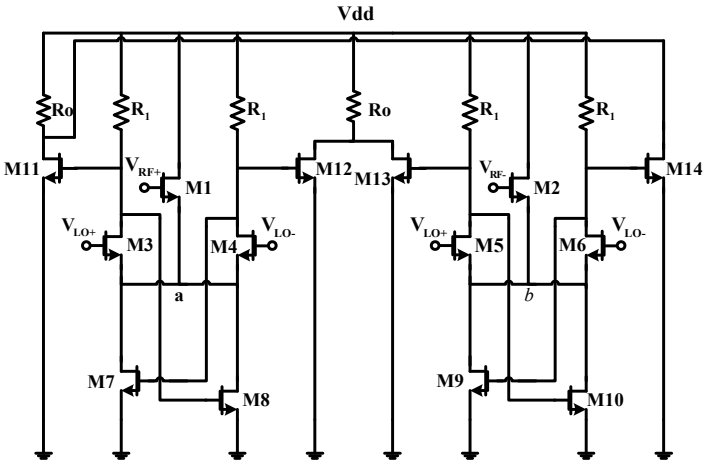


Fig. 1. A low voltage mixer [9]

Besides this, the source of transistors in RF stage is connected to source of transistors in switching stage. Currents I_{M11}, I_{M14}, I_{M12} and I_{M13} which pass through R_0 loads, are summed and produce an output voltage as below:

$$V_{out} = R_0 \left[\left(I_{M11} + I_{M14} \right) - \left(I_{M12} + I_{M13} \right) \right] \quad (2)$$

Assuming that all NMOS transistors are equal having the same parameters, equation (2) yields:

$$V_{out} = -R_0 R_1 k_{n1} k_{n4} \left[\left(V_{LO+} - V_{LO-} \right) \left(V_{RF+} - V_{RF-} \right) \right] \quad (3)$$

Where kn1 and kn4 are transconductance parameter of transistors with LO and RF signal drive, respectively..

B. Improving RF Stage

The complete schematic of the proposed mixer is shown in Fig. 2(a). Employing a PMOS transistor and resistor R in series with the NMOS one make the mixer more linear. In the RF stage, the secondary PMOS transistors are biased in weak inversion and the main NMOS transistors are biased in strong inversion region. Then they have different sign for their second order derivative of g_m.

In order to show how the RF stage in Fig. 2(b) can achieve high IIP3, a Volttera series based analysis of the equivalent circuit, shown in Fig. 2(c), is done.

The Volterra series of the output current can be represented as follows:

$$\begin{aligned} i\left(v_x\right) = {} & C_1\left(S\right) \circ v_x + C_2\left(S_1, S_2\right) \circ v_x^2 \\ & + C_3\left(S_1, S_2, S_3\right) \circ v_x^3 \end{aligned} \quad (4)$$

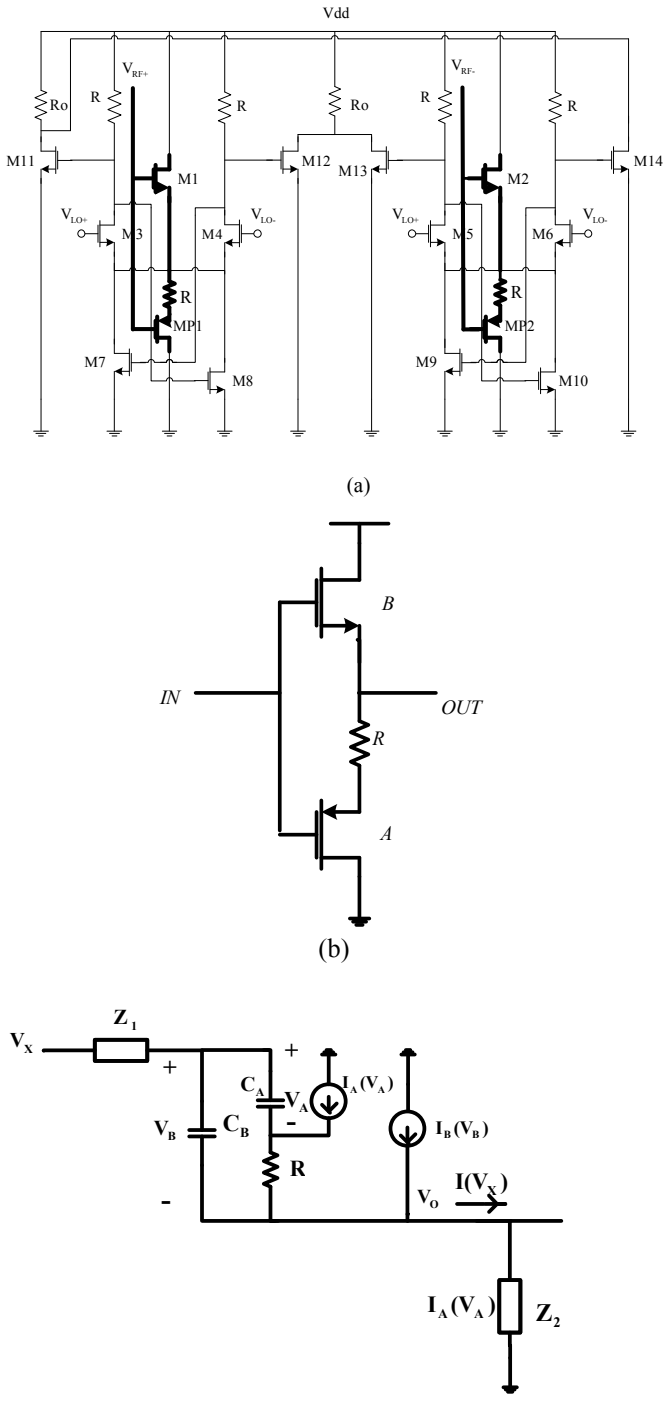


Fig. 2. (a) the proposed highly linear low voltage mixer (b) the improved stage in the proposed mixer (c) equivalent circuit for the proposed RF stage in (b).

Where $C_n(S_1,S_2,\ldots,S_n)$ is nth-order Volterra kernel and by the operator "o", the magnitude and the phase of each v_x^n is changed by the magnitude and phase of $C_n(S_1,S_2,\ldots,S_n)$. The third-order intercept point at $2\omega_b-\omega_a$ (for a two tone excitation at frequencies of ω_b and ω_a) is given by [10]:

$$IP3(2\omega_b-\omega_a)=\sqrt{\frac{4}{3}\left|\frac{C_1(s_a)}{C_3(s_b,s_b,-s_a)}\right|} \tag{5}$$

And, the IIP3 is proportional to square of the above term; consequently, we should minimize the third-order distortion coefficient ($C_3(S_b,S_b,-S_a)$) for IIP3 improvement. According to appendix A, $C_3(S_b,S_b,-S_a)$ can be written as follows:

$$\begin{aligned}C_3(S_b,S_b,-S_a)&=|A_1(S)|^2 A_1(-S)[E(S)+A_1(S)L(S)D(S)\\&+(2M(\Delta S)A_1(\Delta S)+M(2S)A_1(2S))(\frac{G(S)}{3}+\frac{N(S)}{3}A_1(S)L(S))]\end{aligned} \tag{6}$$

Where $A_1(S)$, E(S), L(S) and other coefficients are defined at the appendix.

With some approximation like $g_{1A}\approx 0$ the above expression, can be rewritten as follows:

$$\begin{aligned}C_3(S_b,S_b,-S_a)&=(1-b(S)L(S)A_1(S))\\&\cdot\left[E(S)+\frac{G(S)}{3}(2M(\Delta S)A_1(\Delta S)+M(2S)A_1(2S))\right]\end{aligned} \tag{7}$$

In the above simplified expression, E(S) and G(S) are related to the combination of g_m'' and g_m' of two transistors, respectively:

$$E(S)=(1+SRC_A)g_{3B}+(1+SRC_B+Rg_{1B})g_{3A} \tag{8}$$

$$G(S)=2(1+SRC_A)g_{2B}-2g_{2A}(1+SRC_B+g_{1B}R) \tag{9}$$

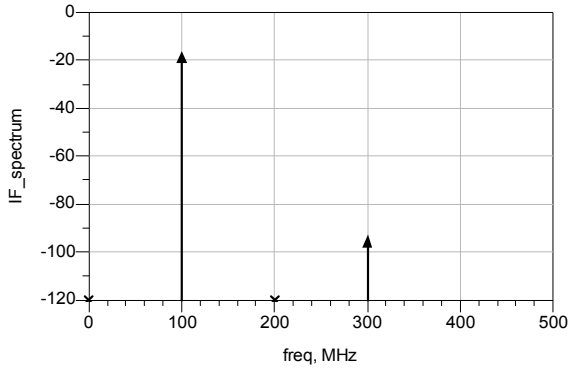
By taking the type of transistors and their operation region in consideration, g_{2A} and g_{2B} have the same sign wile g_{3A} and g_{3B} have opposite sign. Then using appropriate value for resistor R and a suitable size for PMOS transistor make the second term in (7) very small and the third-order distortion decreases significantly.

IV. Simulation Results

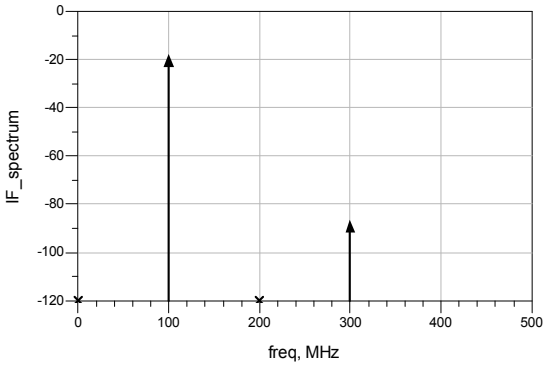
The proposed mixer in Fig. 2(a) simulated in standard TSMC RF CMOS 0.18-µm technology with 1V supply using Advanced Design System (ADS) simulator and is compared with the performance of Low voltage mixer in fig.1.

RF-frequency, LO-frequency and IF-frequency for the structures were considered as 2.4GHz, 2.3GHz and 100MHz, respectively. The LO signal power was selected -10 dBm.

The output spectrum of the mixers for -25 dBm RF input is shown in Fig. 3(a,b). As can be seen, for highly linear mixer the third-order harmonic at 300MHz is 76 dB below the fundamental harmonic at 100MHz.

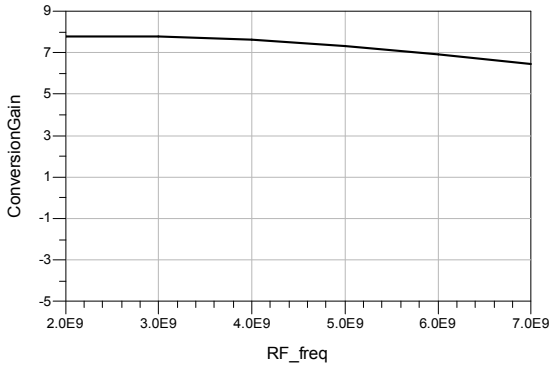


(a)

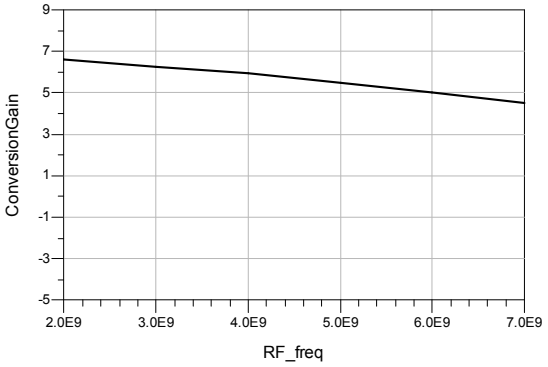


(b)

Fig. 3. Output spectrum for (a) the enhanced mixer in Fig. 2 and (b) mixer in Fig. 1



(a)

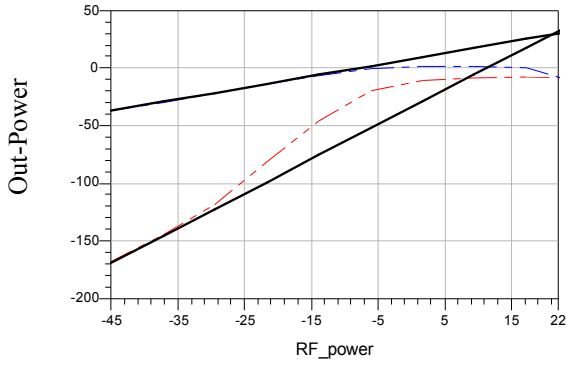


(b)

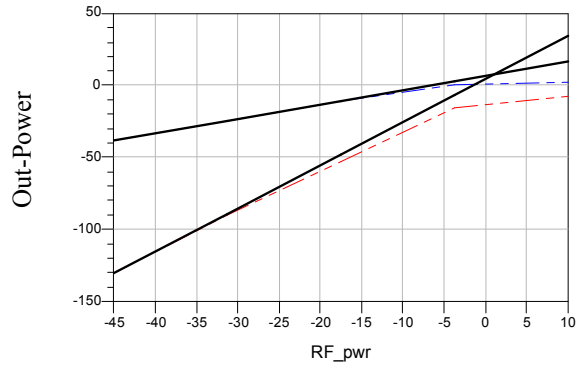
Fig. 4. Conversion gain versus RF frequency for (a) the enhanced mixer in Fig. 2 and (b) mixer in Fig. 1

Table I. Comparison of some CMOS Mixers performance

	Technology (μm)	RF frequency (GHz)	IF frequency (MHz)	Supply Voltage (V)	I (mA)	Conversion Gain (dB)	P-1dB (dBm)	IIP3 (dBm)
[6]	0.18	2.4	100	2	7.4	11.2	-	12.5
[8]	0.18	2.4	10	1	6.6	11	-	4.1
[9]	0.35	0.9	100	1.2	10.67	0.52	-8	1.2
[12]	0.18	2.4	100	3	-	8	-	17.39
[13]	0.18	2.4	100	1.8	4.5	15.7	-	1
[14]	0.18	2.4	50	1.2	5	4	2	8.5
[15]	0.18	3.6	10	1	4.43	4.4	-	5.5
[16]	0.18	2.44	2	1	-	5.3	-7.4	4.6
[17]	0.13	5.5	500	1.2	8	9	-6	2
This work	0.18	2.4	100	1	8.5	7.8	-8	21



(a)



(b)

Fig. 5. Input referred IP3 for (a) the enhanced mixer in Fig. 2 and (b) mixer in Fig. 1

It is shown in Fig. 4(a-b) that Conversion Gain of improved mixer at 2.4GHz RF-frequency is about 7.8 dB while it is about 6.4 dB for the Low voltage mixer in fig.1. The simulated IIP3 of mixers by two input tones with offset is shown in Fig. 5(a-b). The interpolation of two signals indicates IIP3 of 21 dBm and 1 dBm for the highly linear and the Low voltage mixers, respectively, which shows the effectiveness of the proposed technique. In addition, the 1-dB compression point of about -8 dBm is obtained for tow mixer structure from Fig. 5(a,b).

Then by adding some components to the low voltage mixer circuit, we could improve linearity to extremely large value (about 20 dBm increase in IIP3) and the gain is also improved a little. In both structures, a current of 8.52mA is drawn from 1V supply voltage. Therefore, power consumption is similar in both structures since the PMOS is used in weak inversion region that does not influence circuitry current.

Topology presented in Fig. 2(a) is not only comparable to other Gilbert cell based structure for low voltage operation, but also for its better linearity. Table. I summarizes the comparison for performance of the proposed mixer and others. The proposed mixer works at a low supply voltage and has a very good linearity.

V. Conclusion

A low voltage highly linear down conversion mixer is presented. In this work, adjusting the value of a resistor and the aspect ratio of a PMOS transistor at the RF stage of a well known low voltage CMOS mixer, cause an appropriate improvement in the linearity. Also, the Volttera series is used to show how this structure can achieve a high IIP3. As shown in this work, using additional component in RF stage of the mixer can set the amplitude of first and second-order derivative of g_m of transistors so that the IIP3 of mixer achieves to a high value. Using TSMC RF CMOS 0.18-µm technology, the proposed mixer shows an IIP3 of 21 dBm, 1-dB compression point of -8 dBm and 7.8 dB conversion gain. The proposed mixer shows a 20 dBm improvement in IIP3 compared with ones without additional component in RF stage that illustrate the effectiveness of the proposed technique. Furthermore, the proposed structure does not impose additional power and area consumption, and this can be stated as its positive points.

VI. Appendix

The relation between gate-source voltages of two transistors in Fig. 2 (c) is:

$$\begin{aligned} v_B &= v_A + R(i_A + SC_A V_A) = Ri_A + V_A(1+SRC_A) \\ &= Ri_A + F(S)V_A \end{aligned} \quad (A.1)$$

Relation between the current of transistors and gate-source voltage of v_A :

$$\begin{aligned} i_A &= -\left(g_{1A}(-v_A) + g_{2A}(-v_A)^2 + g_{3A}(-v_A)^3\right) \\ &= g_{1A}v_A - g_{2A}v_A^2 + g_{3A}v_A^3 \end{aligned} \quad (A.2)$$

$$\begin{aligned} i_B &= g_{1B}v_B + g_{2B}v_B^2 + g_{3B}v_B^3 = g'_{1B}V_A + g'_{2B}V_A^2 + g'_{3B}V_A^3 \\ &\quad + g_{1B}Ri_A + g_{2B}(Ri_A)^2 + g_{3B}(Ri_A)^3 \end{aligned} \quad (A.3)$$

$$\begin{aligned} i(v_x) &= i_A + i_B + v_B SC_B + v_A SC_A \\ &= i_B + i_A(1+SRC_B) + V_A(SC_A + F(S)SC_B) \end{aligned} \quad (A.4)$$

The gate-source voltage of v_A can be modeled by the following Volterra serie in terms of voltage v_x :

$$v_A = A_1(S)\circ v_x + A_2(S_1,S_2)\circ v_x^2 + A_3(S_1,S_2,S_3)\circ v_x^3 \quad (A.5)$$

Using (A.2), (A.3) and (A.5) in (A.4) and comparing it with

(4), the following expression is obtained:

$$C_1(S)=\left(g'_{1B}+g_{1A}(1+SRC_B+Rg_{1B})+F(s)\times SC_B+SC_A\right)A_1(S) \quad \text{(A.6)}$$

$$\begin{aligned}&C_3(S_1,S_2,S_3)=(g'_{3B}+g_{3A}(1+SRC_B+Rg_{1B})\\&-2g_{2B}R^2g_{1A}g_{2A}+g_{3B}R^3g_{1A}^3)A_1(S_1)A_1(S_2)A_1(S_3)\\&+\left(g'_{1B}+g_{1A}(1+\mathrm{SRC_B}+g_{1B}R)\right)A_3(S_1,S_2,S_3)\\&+2\left(g'_{2B}-g_{2A}(1+SRC_B+g_{1B}R)+g_{2B}R^2g_{1A}^2\right)\overline{A_1(S_1)A_2(S_2,S_3)}\\&=\mathrm{E(S)}A_1(S_1)A_1(S_2)A_1(S_3)+L(S)A_3(S_1,S_2,S_3)+G(S)\overline{A_1(S_1)A_2(S_2,S_3)}\end{aligned} \quad \text{(A.7)}$$

Where

$$\overline{A_1(S_1)A_2(S_2,S_3)}=\frac{1}{3}\left[A_1(S_1)A_2(S_2,S_3)+A_1(S_2)A_2(S_1,S_3)+A_1(S_3)A_2(S_1,S_2)\right] \quad \text{(A.8)}$$

To find $C_1(S)$ and $C_3(S_1,S_2,S_3)$, we first need to find $A_1(S)$, $A_2(S_1,S_2)$ and $A_3(S_1,S_2,S_3)$.

The KCL equations for fig.2(c) are as below:

$$\frac{v_1-v_x}{Z_1}+\left(SC_A+F(S).SC_B\right)v_A+SRC_Bi_A=0 \quad \text{(A.9)}$$

$$v_A\left(F(s)\times SC_B+SC_A\right)+(1+SRC_B)i_A+i_B-\frac{v_o}{Z_2}=0 \quad \text{(A.10)}$$

On the other hand:

$$v_1-v_o=v_B=F(S)V_A+R.i_A \quad \text{(A.11)}$$

Considering three expressions of (A.9), (A.10) and (A.11), the unknown parameter v_A is obtained:

$$\begin{aligned}v_A=&\frac{1}{F(S).(1+SC_B(Z_1+Z_2))+SC_A(Z_1+Z_2)/(SC_A+F(S).SC_B)}\\&.[v_x+(Z_1+F(S)/(SC_A+F(S).SC_B))i_B\\&+(-R+(1+SRC_B).F(S)/(SC_A+F(S).SC_B))+Z_1)i_A]\end{aligned} \quad \text{(A.12)}$$

For ease of using (A.12), it is rewritten as follows:

$$v_A=\frac{v_x-b(S)i_B-a(S).i_A}{Y(S)} \quad \text{(A.13)}$$

Where

$$b(S)=-Z_1-F(S)/(SC_A+F(S).SC_B) \quad \text{(A.14)}$$

$$a(S)=-(-R+Z_1)-(1+SRC_B).F(S)/(SC_A+F(S).SC_B) \quad \text{(A.15)}$$

$$Y(S)=\frac{F(S).(1+SC_B(Z_1+Z_2))+SC_A(Z_1+Z_2)}{Z_2(SC_A+F(S).SC_B)} \quad \text{(A.16)}$$

Parameters i_A and i_B in (A.13) can be replaced by (A.2) and (A.3), respectively. Then, using (A.5) in the resulted expression, the unknown parameters $A_1(S)$, $A_2(S_1,S_2)$ and $A_3(S_1,S_2,S_3)$ can be calculated. To find $A_1(S)$, v_x is replaced with e^{St}. Equalizing the coefficients of e^{St} on both sides in (A.13) and solving for $A_1(S)$, we get:

$$A_1(S)=\frac{1}{Y(S)+b(S)g'_{1B}+g_{1A}(a(S)+b(S)Rg_{1B})} \quad \text{(A.17)}$$

To find $A_2(S_1,S_2)$, v_x is replaced with $e^{S_1t}+e^{S_2t}$. Equalizing the coefficients of $e^{S_1t+S_2t}$ on both sides in (A.13) and solving for $A_2(S_1,S_2)$, we get:

$$\begin{aligned}A_2(S_1,S_2)=&\frac{(a(S)+b(S)Rg_{1B})g_{2A}-b(S)g'_{2B}-b(S)g_{2B}R^2g_{1A}^2}{Y(S)+b(S)g'_{1B}+g_{1A}(a(S)+b(S)Rg_{1B})}\times A_1(S_1)A_1(S_2)\\&=\left[(a(S)+b(S)Rg_{1B})g_{2A}-b(S)g'_{2B}-b(S)g_{2B}R^2g_{1A}^2\right]\times A_1(S_1)A_1(S_2)A_1(S_1+S_2)\\&=\mathrm{M(S)}\times A_1(S_1)A_1(S_2)A_1(S_1+S_2)\end{aligned} \quad \text{(A.18)}$$

Similarly, $A_3(S_1,S_2,S_3)$ can be derived as:

$$\begin{aligned}A_3(S_1,S_2,S_3)=&[(-2b(S)g'_{2B}+2g_{2B}R^2g_{1A}^2+2g_{2A}(a(S)+b(S)g_{1B}R)\overline{A_1(S_1)A_2(S_2,S_3)}\\&+(b(S)g'_{3B}-g_{3A}(a(S)+b(S)g_{1B}R)+2b(S)g_{2B}R^2g_{1A}g_{2A}-b(S)g_{3B}R^3g_{1A}^3\\&+3b(S)g_{1A}^2g_{2A}g_{3B}R^3)A_1(S_1)A_1(S_2)A_1(S_3)]\times A_1(S_1+S_2+S_3)\\&=A_1(S_1+S_2+S_3)\times[N(S)\overline{A_1(S_1)A_2(S_2,S_3)}+D(S)A_1(S_1)A_1(S_2)A_1(S_3)]\end{aligned} \quad \text{(A.19)}$$

It can be founded from (A.19) that second order distortion participates in forming third-order distortion, too.

Exciting the circuit with vx=A[cos(ω_at)+cos(ω_bt)], third-order distortion at $2\omega_b-\omega_a$, is found with replacement of S_1 and S_2 by S_a and S_3 by S_b. It is assumed that the frequencies are close together and approximately equal ($S_a\approx S_b\approx S$)), then:

$$\begin{aligned}&A_3(S_b,S_b,-S_a)=A_1(S)\times\\&[N(S)\overline{A_1(S_b)A_2(S_b,-S_a)}+D(S)\left|A_1(S)\right|^2A_1(-S)]\end{aligned} \quad \text{(A.20)}$$

Where

$$\overline{A_1(S_b)A_2(S_b,-S_a)}=\frac{1}{3}\left[2A_1(S_b)A_2(S_b,-S_a)+A_1(-S_a)A_2(S_b,S_b)\right] \quad \text{(A.21)}$$

Considering (A.19), the above equation is obtained as follows:

$$\begin{aligned}\overline{A_1(S_b)A_2(S_b,-S_a)}=&\frac{1}{3}[2A_1(S)M(\Delta S)A_1(S)A_1(-S)A_1(\Delta S)\\&+A_1(-S)M(2S)A_1(S)A_1(S)A_1(2S)]\\&=\frac{1}{3}\left|A_1(S)\right|^2A_1(-S)[2M(\Delta S)A_1(\Delta S)+M(2S)A_1(2S)]\end{aligned} \quad \text{(A.22)}$$

Where $\Delta S=S_b-S_a$ and ΔS can be set to zero if it is assumed that $S_a\approx S_b$. Considering (A.22) and (A.20), the following expression is obtained for $A_3(S_1,S_2,S_3)$:

$$A_3(S_b,S_b,-S_a)=|A_1(S)|^3 A_1(-S)\times \left[\frac{N(S)}{3}(2M(\Delta S)A_1(\Delta S)+M(2S)A_1(2S))+D(S)\right] \quad \text{(A.23)}$$

And by considering (A.6), (A.22) and (A.23) the $C_3(S_1,S_2,S_3)$ is concluded as follows:

$$C_3(S_b,S_b,-S_a)=|A_1(S)|^2 A_1(-S)[E(S)+A_1(S)L(S)D(S)+ (2M(\Delta S)A_1(\Delta S)+M(2S)A_1(2S))(\frac{G(S)}{3}+\frac{N(S)}{3}A_1(S)L(S))] \quad \text{(A.23)}$$

As can be seen in the Fig. 2 the impedance of Z_2 is related to the impedance in the output node that is approximately related to gate-source capacitance of transistors in switching stage.

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