A 12b 100MS/s Highly Power Efficient Pipelined ADC for Communication Applications

Seyed Alireza Zahrai, Seyed Javad Azhari

***Abstract*—A 12 bits 100 MS/s pipelined ADC with a high ENOB is proposed for communication applications especially for Wireless Networks. The proposed ADC achieves low power, high resolution and high speed operation due to deliberately design of a low power high performance operational amplifier for the pipeline stages. In addition, more power reduction is achieved by proper power and parameters scaling for the stages granting the proposed ADC remarkably distinguished power efficiency compared to other ones. The ADC has been designed and simulated by HSPICE in 0.18 µm CMOS technology. It achieves such other merits as 73 dB signal to noise and distortion ratio (SNDR), 87.1 dB spurious free dynamic range (SFDR) and 11.8 effective number of bits (ENOB). The overall ADC consumes 58 mW and uses a 1.8 V supply.**

***Index Terms*—Analog to Digital Conversion (ADC), high resolution, low power, high speed, power efficient, pipelined analog-to-digital converter, Switched capacitor**

I. Introduction

ANALOG to digital converters are one of the essential elements in Mixed-Signal circuits and systems especially communication systems. Among different types of ADCs, pipelined ADCs are commonly used for medium to high resolution and speed data conversions, with low power consumption. Pipelined ADCs are used in such wide applications as wired or wireless communication systems, digital imaging, ultrasound medical imaging, digital video broadcasting, DSL networks and HD TVs. These days, pipelined ADCs are widely used in wireless communication systems which demand high resolution and high speed data conversions [1]. In portable communication circuits and systems which use battery as the power supply, the amount of power consumption is a critical necessity, thus, designing a low power pipelined ADC becomes more important.

Nowadays by decreasing the feature size of transistors in modern technologies and sharp increase of the number of devices on a single chip, low power and low voltage design have become a common mandatory. Thus, two main reasons for reducing voltage and power are: constraints imposed by modern technology and development of portable devices for communications like space bases and mobile phones, consumer electronics as laptops and mp3 players, and medical devices that are implanted in human body.

Many techniques and innovations have been proposed so far to design high resolution and high speed pipelined ADCs, among which reducing the power consumption is always a challenging issue. To increase the accuracy some techniques like capacitor error averaging [2] and offset cancellation [3] have been proposed, but they limit the high speed operation. Also, calibration techniques are commonly used in pipelined ADCs design to achieve high resolution plus high sampling rate, but they increase the power consumption, design complexity and the die area [4-5].

The popular methods to reduce the power consumption of a pipelined ADC are stage power scaling [4], [6] and per-stage resolution optimization [7]. To achieve more power saving, other techniques like op amp sharing [8-9] and switched-opamp techniques [10-11] have been proposed. However, these techniques can not be used for high-speed high-resolution ADCs due to such drawbacks as memory effects [8] and limited sampling rate [10]. Another alternative to meet low power at high resolution and high speed is using circuit design techniques to create more power efficient operational amplifiers topologies [12-13].

In this work, a 12 bits 100 MS/s calibration-free pipelined ADC is presented which is more power efficient (Power per Sample) than some other advanced works in the same field. It benefits from optimum stage scaling and a two-stage opamp deliberately designed towards high performance and low power consumption. The opamp is the key element of a pipelined ADC, because it is the major power hungry element and confines the overall resolution and speed of the ADC [4], [14]. A low power two-stage cascode-compensated opamp with class AB output stages is designed to make high resolution and high speed operation possible.

This paper is organized as follows. Section II describes the block diagram and overall architecture of the proposed ADC, reviews the 1.5 bit switched capacitor pipelined stage architecture and explains its main advantages and challenges. Section III describes the proposed opamp and other circuit implementations. Section IV presents the accurate simulation results of the proposed pipelined ADC and Section V draws a

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conclusion of the work.

II. Pipelined ADC Architecture

A. Proposed Pipelined ADC

The proposed 12 bits pipelined ADC uses 1.5 bit per Stage architecture and consists of ten 1.5b stages and one 2b flash ADC as the final stage. The total ADC is shown in Fig.1. It consists of delay elements (set of shift registers) used for bit alignment and a digital correction block (a digital adder) that produces the final 12 bits in the output.

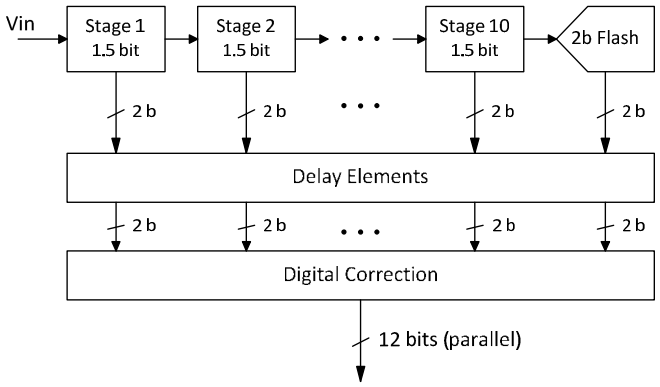

Fig. 1. Block diagram of the proposed pipelined ADC

Each pipeline stage has two important tasks: first, producing its output bits, and second, generating the residue voltage to deliver to the next stage. The block diagram of a pipeline stage is shown in Fig. 2. As a common expression, the set of DAC, subtractor and gain block, are named Multiplying Digital to Analog Converter (MDAC). In this work we use opamp based switched capacitor (SC) architecture to implement the MDAC.

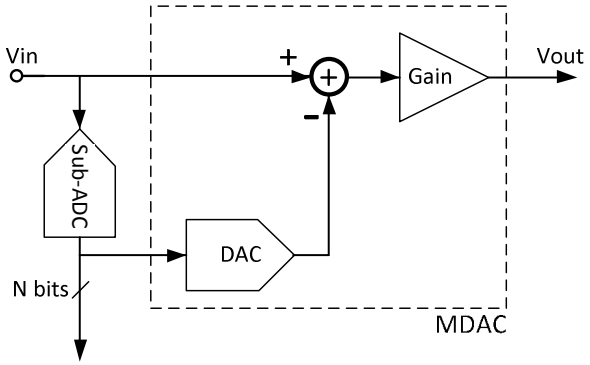

Fig. 2. Block diagram of a pipeline stage

B. 1.5 Bit Pipeline Stage

Using redundancy in the stages is a popular method to increase the accuracy of a pipelined ADC [3], [5], [9], [15]. Similarly, in the proposed ADC we use 1.5b per stage architecture to achieve better accuracy.

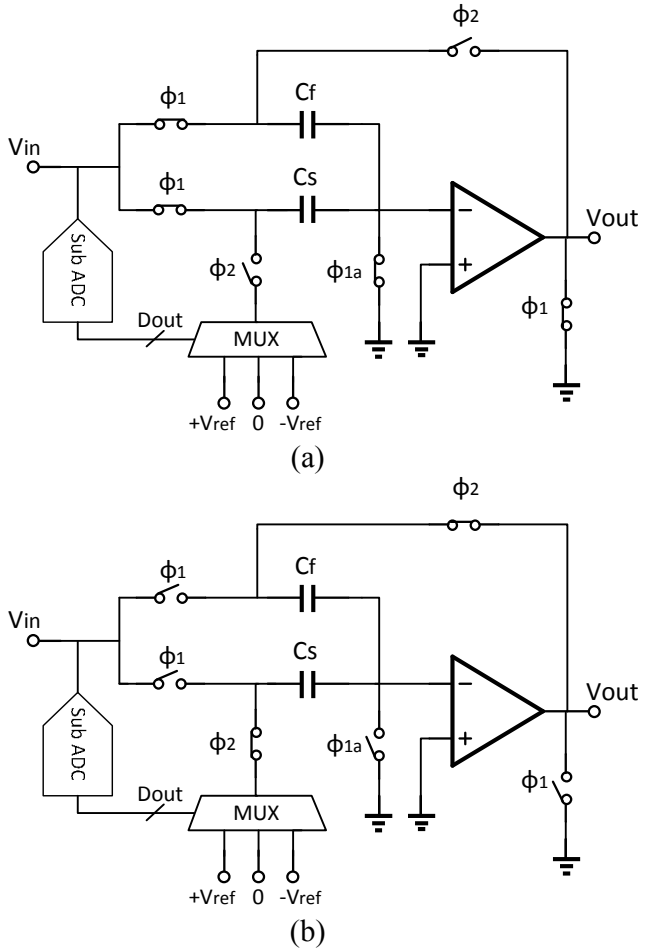

Fig. 3. Operation of a SC 1.5bit pipelined stage (a) Sampling phase, (b) Amplifying phase.

The 1.5b stage works with a 2 phase non-overlapping clock, the sampling and the amplifying phases. As shown in Fig. 3, during the sampling phase (ϕ_1 is high) the input voltage signal is sampled by the sampling capacitors C_s and C_f, and also the input voltage is applied to the sub-ADC. Consequently, the output bits of the stage are generated at this phase. The ϕ_{1a} is for ensuring that bottom plate sampling is performed, because bottom plate sampling remarkably reduces the signal dependent charge injection on the sampling capacitors [16]. In the amplification phase, Fig. 3 (b), ϕ_2 is high, C_f is located in a feedback loop with the opamp. Based on the sub-ADC's output bits, the output of the analog MUX is selected and the positive plate of C_s connects to the output of the analog MUX. As a result, in this phase the residue of the current stage is produced and becomes ready to deliver to the next pipeline stage. This residue voltage (Vout) is calculated by equation (1) [15].

$$V_{out}=\begin{cases}\left(1+\dfrac{C_s}{C_f}\right)V_{in}-\dfrac{C_s}{C_f}V_{\mathrm{Ref}} & ,\ \text{if}\ \ V_{in}>V_{\mathrm{Ref}}/4\\ \left(1+\dfrac{C_s}{C_f}\right)V_{in} & ,\ \text{if}\ \ -V_{\mathrm{Ref}}/4<V_{in}<V_{\mathrm{Ref}}/4\\ \left(1+\dfrac{C_s}{C_f}\right)V_{in}+\dfrac{C_s}{C_f}V_{\mathrm{Ref}} & ,\ \text{if}\ \ V_{in}<-V_{\mathrm{Ref}}/4\end{cases} \quad (1)$$

In a 1.5bit pipeline stage the gain of two is needed to generate the proper input for the next stage. That follows $C_f = C_s$, thus the ideal output (residue) of a 1.5bit stage and its output bits are calculated by equation (2).

$$V_{out}=\begin{cases}2V_{in}-V_{\mathrm{Ref}} & \text{and}\ \mathrm{D}_{out}=10,\ \text{if}\ \ V_{in}>V_{\mathrm{Ref}}/4\\ 2V_{in} & \text{and}\ \mathrm{D}_{out}=01,\ \text{if}\ \ -V_{\mathrm{Ref}}/4<V_{in}<V_{\mathrm{Ref}}/4\\ 2V_{in}+V_{\mathrm{Ref}} & \text{and}\ \mathrm{D}_{out}=00,\ \text{if}\ \ V_{in}<-V_{\mathrm{Ref}}/4\end{cases} \quad (2)$$

The sub-ADC block which is not shown in details, consists of 2 comparators and one encoder block. It compares the input voltage with 2 voltage levels ($-V_{\mathrm{ref}}/4$ and $V_{\mathrm{ref}}/4$), generates output bits and commands the MUX (DAC) to choose the proper voltage.

The 1.5 bit per stage architecture has two main advantages: First, the comparator offset can be up to $V_{ref}/4$, where V_{ref} is the maximum peak voltage of the input [17]. Second, since the difference between input applied to MDAC and sub-ADC is less than $V_{ref}/4$, the effect of sampling skew appears as an offset in the input of the sub-ADC comparator, which is eliminated by the redundancy of the first 1.5b stage [4]. Thus the demand of using a front-end sample and hold (S/H) is eliminated due to the redundancy of the first pipelined stage and favorably the power consumption and die area of the ADC are reduced.

In the ADCs, fully differential analog signals are preferred to get a better power supply rejection and immunity to common mode noise [14]. Thus, in this paper we use fully differential architecture for MDAC which is shown in Fig. 4.

C. Non-Idealities

There are three main considerations in designing a 1.5 bit pipeline stage:

First, to achieve the desired linearity for the overall ADC, a precise gain of 2 is needed for each stage. Since this gain is determined by the capacitors ratio C_s/C_f the mismatch between capacitors becomes important. This problem can be alleviated by capacitor trimming methods [15] and capacitor error averaging [2]. Also, the mismatch depends on the technology used in fabrication. For a specific CMOS technology, as a general principle, increasing the size of capacitors decreases the percent of mismatch and consequently increases the overall linearity. On the other hand, increasing the capacitors sizes will decrease the overall sampling speed of the ADC, brings up a tradeoff between the linearity and the ADC sampling speed.

Second, the DC gain of the opamp must be high enough to reduce the finite gain error. Neglecting the other non-idealities, in an N bit pipelined ADC; it has been shown that the simplified constraint of relation (3) exists for the amplifier gain of the first stage [4]:

$$A > 2^N \quad (3)$$

Consequently, an amplifier with a large open loop DC gain is required when designing an opamp based SC circuit to implement a pipeline stage for the medium to high resolution pipelined ADC.

Third, the settling time of the opamp limits the overall pipelined ADC performance. In order to have an opamp sufficiently settled in the amplifying clock phase, the opamp must have enough bandwidth. Similar to the high gain, an opamp with a large bandwidth consumes more power. So, to minimize the power consumption we should optimize the bandwidth of the opamp.

In this work, the design constraints for power scaling of the stages have been considered. The scaling of parameters and power is performed according to the importance of the stages which is lessened from the first stage to the last one [15].

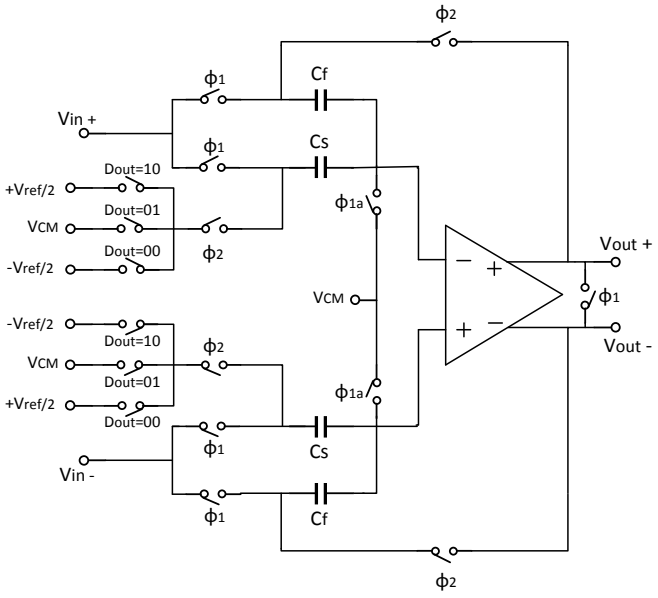

Fig. 4. Fully Differential implementation of the 1.5 bit switched capacitor pipelined stage's MDAC

III. CIRCUIT IMPLEMENTATION

To obtain the desired performance for the proposed ADC we have used circuit design techniques to design optimized blocks for the proposed ADC.

A. Operational Amplifier

The operational amplifier is the key element of the MDAC in a switched capacitor pipeline stage. In practice it is the most power consuming block in each stage. In addition, the overall resolution and speed of the ADC is limited to the op amps of the stages. Thus, opamp is the bottle neck of opamp based switched capacitor pipelined ADC design and designing a high performance and low power opamp has a significant importance.

A high resolution, high speed pipelined ADC requires an amplifier with a very large open loop DC gain, a wide bandwidth, and fast settling /high slew rate. The common way to achieve this requirement is using one stage op amps like telescopic and folded ones with gain boosting [2], [3], [5]. But the main drawbacks of these topologies are limited signal swing and intricate settling behavior because of the regulating amplifiers. Another alternative is using multi-stage amplifiers which have a high open loop DC gain. However, due to compensation there is a tradeoff between the stability and bandwidth of this alternative type [14].

The proposed opamp is shown in Fig. 5. It consists of a telescopic-cascode amplifier [18] as its first stage and a class AB output stage.

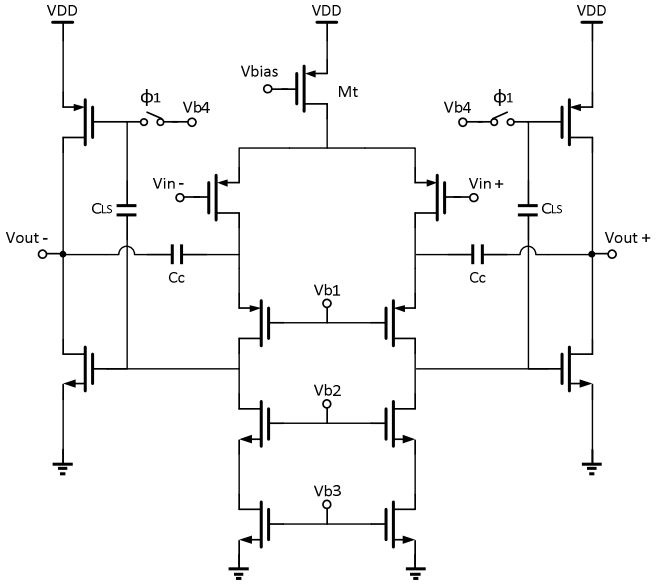

Fig. 5. Schematic of the proposed Fully Differential Operational amplifier

A class AB stage can lead to lower power consumption and high output swing operation [19]. We utilize the introduced method in [20] to the class AB output stage of the designed opamp in order to achieve the high slew rate required. The switch and C_{LS} capacitor which are added to the output stage can increase the output current, dependently to the signal, instead of using a constant bias voltage for the PMOS in the output stage. More current crossing through the output load leads to a higher slew rate and quicker settling time.

Applying cascode compensation to a two stage operational amplifier leads to less power consumption rather than Miller compensation while preserves its fast settling behavior [21]. Thus to meet the required stability and settling behavior preserving low power operation, a cascode compensation method is used by locating C_C between two stages of the opamp.

The opamp for the first pipeline stage, which is the most critical stage, is designed to achieve 86dB gain and 800MHz bandwidth. As another strongly effective plan, to reduce the overall ADC power consumption, applying scaling method, the opamps of the next stages are deliberately designed with lower gains and bandwidths.

B. CMFB

For a more properly operation, fully differential op amps are also equipped with common mode feedback (CMFB) circuit that modifies the common mode voltage variations in the output and stabilizes the output dc level (output common mode) at a desired voltage [16]. In this work we have used a conventional SC CMFB circuit which is shown in Fig. 6. In this circuit Vctrl is applied to a current source, the current of which is added to the current of the tail current source and makes the output to be stable in a preferred interval. To avoid nonlinearity problems, transmission gates are used as the switches which are directly connected to the output voltage.

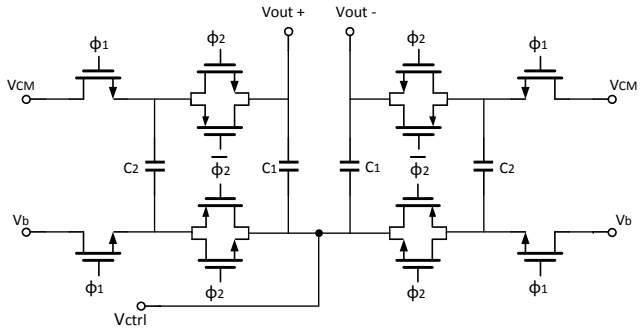

Fig. 6. SC CMFB circuit

C. Comparator

In this work, a fully differential static comparator is designed to satisfy the required high resolution. The designed comparator is shown in Fig. 7. It compares $(V_{in+} - V_{in-})$ with $(V_{ref+} - V_{ref-})$ and resets when ϕ_2 becomes high. The output inverters are for generating definite low and high voltage levels. Dynamic comparators have low power consumption,

but they are not suitable for medium to high resolution pipelined ADCs [14].

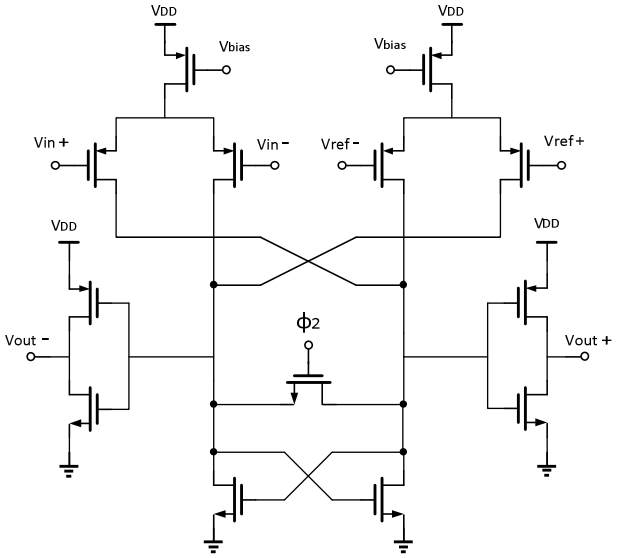

Fig. 7. Schematic of the Differential pair Comparator

IV. Simulation Results

The proposed ADC is designed in TSMC 0.18 µm CMOS technology and simulated with HSPICE. The ADC uses 1.8V as the voltage supply and its input voltage range is 2Vpp.

The Total power consumption of the proposed ADC is 58mW which is accounted as a quite low power amongst opamp based pipelined ADCs with a similar performance.

Figs. 8 and 9, show DNL and INL plot of the proposed ADC respectively. DNL of the ADC is +0.65 LSB (Max) and its INL is +1.2 LSB (Max).

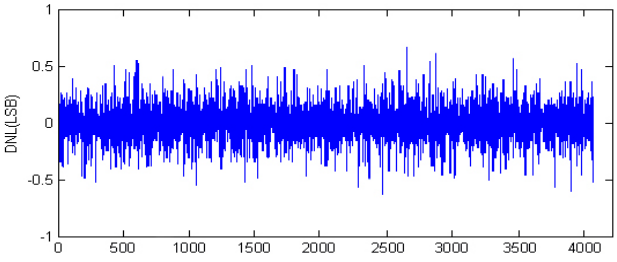

Fig. 8. ADC DNL plot

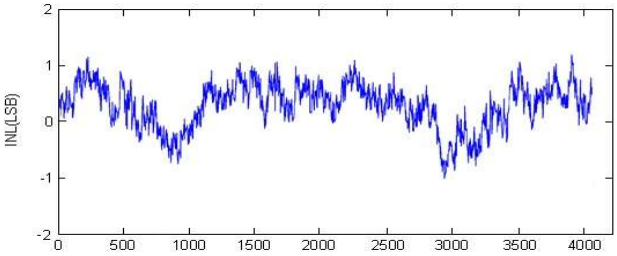

Fig. 9. ADC INL plot

The FFT plot of the ADC output with fin=10.3 MHz and sampling rate of 100MS/s is shown in Fig. 10. From the plot the ADC SNDR is 73 dB which leads to 11.8 ENOB. The SFDR in this condition equals to 87.1 dB.

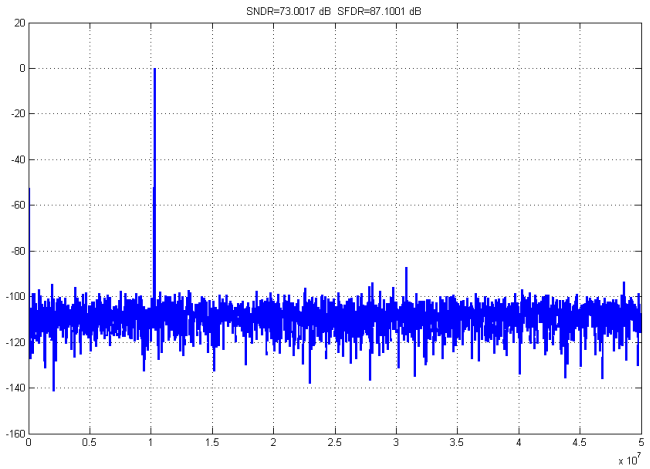

Fig. 10. FFT plot of ADC output for Fin=10.3 MHz @ Fs=100MS/s

To evaluate the ADC dynamic performance at full Nyquist rate, the FFT plot of the ADC output with fin=49.1 MHz and sampling rate of 100MS/s is shown in Fig. 11. From the plot the ADC SNDR is 69.2 dB which gives 11.2 ENOB, and SFDR equals to 87.5 dB. These results ensure us that the ADC completely satisfies the desired performance.

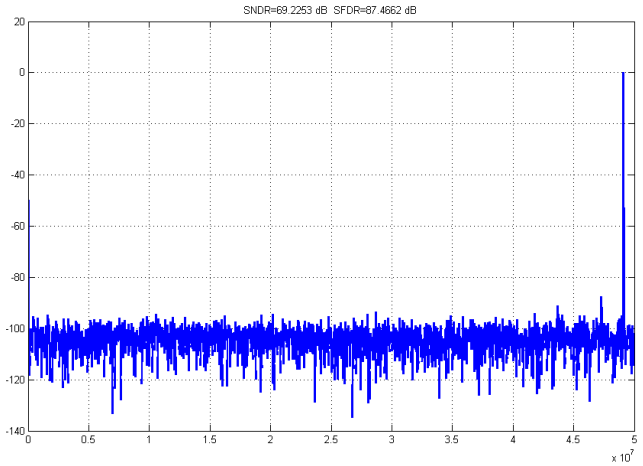

Fig. 11. FFT plot of ADC output for Fin=49.1 MHz @ Fs=100MS/s

To perform a fair evaluation of the proposed ADC performance compared to other works, we use the conventional definition of figure of merit (FOM) [4], [5]:

$$FOM = \frac{Power}{2^{ENOB}.F_s}$$

In this definition the lower FOM means better performance. The FOM of this work is 0.16 pJ/Sample which is the lowest FOM among its counterparts. The proposed ADC performance is compared with those of similar ones in Table 1. As is shown in Table 1, the proposed ADC achieves the same high resolution with a high sampling rate while performs the best ENOB and FOM among others.

TABLE I
COMPARISON TABLE

	[22]	[23]	This work
Resolution	12 bits	12 bits	12 bits
Sampling Rate	40 MS/s	110 MS/s	100 MS/s
ENOB	10.4	10.4	11.8
SNDR	64.5 dB	64.2 dB	73 dB
SFDR	70.5 dB	69.4 dB	87.1 dB
DNL	0.3 LSB	1.2 LSB	0.65 LSB
INL	0.4 LSB	1.5 LSB	1.2 LSB
FOM	3.9 pJ/Sample	0.65 pJ/Sample	0.16 pJ/Sample
Technology	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Voltage Supply	1.8 V	1.8 V	1.8 V
Input Voltage Swing	N/A	2 Vpp	2 Vpp
Power	210 mW	97 mW	58 mW

V. CONCLUSION

A low power 12 bits 100MS/s pipelined ADC in 0.18 µm CMOS technology is proposed in this paper. This ADC is designed in 1.5 bit per stage architecture without using calibration methods. Also, due to the redundancy in output bits of the first stage, there is no need to a front end S/H circuit, causing the overall power and circuitry to be greatly reduced. With optimized design of a low power two stage operational amplifier and stages power scaling, the ADC achieves high resolution and high speed while preserving very good static and dynamic performance. Also, the proposed ADC consumes a comparatively low power which makes it more important when is used in portable instruments and systems. An ADC with such performance can be utilized in such many applications as wired and wireless communications, biomedical, imaging, and instrumentation. The proposed ADC can be especially used in the wireless communication systems.

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