Reconfigurable Optimized WCDMA DDC for Software Defined Radios

Rajesh Mehra

Abstract*— In this paper an optimized approach is presented to design & implement WCDMA based digital down converter for *S*oftware Defined *R*adios. The proposed DDC is designed using Park McClellan algorithm to achieve optimal filter order for hardware reduction. A computationally efficient polyphase decomposition structure is presented to enhance the speed and area efficiency. The embedded multipliers and LUTs of target FPGA have been efficiently utilized to enhance the system performance. The proposed DDC model is designed with Matlab, synthesized with Xilinx Synthesis Tool (XST) and implemented on Virtex-II Pro based xc2vp30-7ff896 FPGA device. The results show that proposed design can operate at a maximum frequency of 145.54 MHz by consuming 0.10313W power at 25° C junction temperature. The multiplier based FPGA has been used for hardware implementation to provide cost effective solution for SDR based wireless applications.

***Index Terms*—3 G Mobile Communication, Digital Filters, Software radio, Radio Frequency.**

I. NTRODUCTION

Today's consumer electronics such as cellular phones and other multi-media and wireless devices often require digital signal processing (DSP) algorithms for several crucial operations in order to increase speed, reduce area and power consumption. The range of user terminals that need to be connected in this communication world, include cell phones, video phones, satellite phones, PDAs, portable computers and other nomadic computing devices [1]. To flourish and succeed in this dynamic environment, suppliers must build highly flexible systems that operate across multiple wireless and wired network standards. They must be able to rapidly adopt new business models as they evolve, and they must be able to incorporate new signal processing techniques that allow increased network capacity, increased coverage, increased quality of service, or a combination of all. The answer to the diverse range of requirements is *software defined radio*. The digital signal processing application by using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates. It allows partitioning of the high-speed processing into parallel multiple lower speed processing tasks which can lead to a significant saving in computational power and cost [2].

Due to a growing demand for such complex DSP applications, high performance, low-cost Soc implementations of DSP algorithms are receiving increased attention among researchers and design engineers. Although ASICs and DSP chips have been the traditional solution for high performance applications, now the technology and the market demands are looking for changes. On one hand, high development costs and time-to-market factors associated with ASICs can be prohibitive for certain applications while, on the other hand, programmable DSP processors can be unable to meet desired performance due to their sequential-execution architecture. In this context, embedded FPGAs offer a very attractive solution that balance high flexibility, time-to-market, cost and performance [3].

The widespread use of digital representation of signals for transmission and storage has created challenges in the area of digital signal processing. The applications of digital FIR filter and up/down sampling techniques are found everywhere in modem electronic products. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost. There are many applications where the sampling rate must be changed. Interpolators and decimators are utilized to increase or decrease the sampling rate. Up sampler and down sampler are used to change the sampling rate of digital signal in multi rate DSP systems. This rate conversion requirement leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter should be placed to attenuate these errors.

A digital down convertor (DDC) is an important part of SDR based 3G or 4G baseband receivers. It shifts the spectrum of interest from its carrier frequency, i.e. intermediate frequency to baseband. It also performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR). A DDC is mainly used to down convert or decimate the GSM signal. Typically low pass filters are used to reduce the bandwidth of a signal prior to reducing the sampling rate. This is done to minimize aliasing due to the reduction in the sampling rate. Down sampler is basic

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sampling rate alteration device used to decrease the sampling rate by an integer factor [4]-[6]. On the receiver side, digital IF techniques can be used to sample an IF signal and perform channelization and sample rate conversion in the digital domain. Using under sampling techniques, high frequency, IF signals typically more than 100MHz can be quantified. For SDR applications, since different standards have different chip/bit rates, non-integer sample rate conversion is required to convert the number of samples to an integer multiple of the fundamental chip/bit rate of any standard.

There are many advanced signal processing tasks performed in a modern digital receiver using two sub-systems called front end and back end systems. A front-end sub system operates at high-data rate and a back-end operates at low data rate or chip-rate. The front-end high-data rate FPGA DSP implements channelization functions for a multi-carrier system. Each channelizer accesses the digital IF (intermediate frequency), translates a channel to baseband and using a multi-stage multi-rate filter adjusts the sample rate to satisfy Nyquist for the selected band. The back-end processor will typically operate on multiple slower rate sample streams performing functions like rake processing, adaptive rake processing, demodulation, turbo decoding, Viterbi decoding. In a QAM system, carrier recovery, timing recovery and adaptive channel equalization will be required. Virtually all digital receivers perform channel access using a digital down-converter (DDC). A DDC is mainly consists of decimators and RRC or pulse shaping filters.

Pulse shaping filters are used at the heart of many modern data transmission systems like mobile phones, HDTV, SDR to keep a signal in an allotted bandwidth, maximize its data transmission rate and minimize transmission errors. The ideal pulse shaping filter has two properties:

i. A high stop band attenuation to reduce the inter channel interference as much as possible.
ii. Minimized inter symbol interferences (ISI) to achieve a bit error rate as low as possible.

The RRC filters are required to avoid inter-symbol interference and constrain the amount of bandwidth required for transmission. Root Raised Cosine (RRC) is a favourable filter to do pulse shaping as it transition band is shaped like a cosine curve and the response meets the Nyquist Criteria. The first Nyquist criterion states that in order to achieve an ISI-free transmission, the impulse response of the shaping filter should have zero crossings at multiples of the symbol period [7]. A time-domain sinc pulse meets these requirements since its frequency response is a brick wall but this filter is not realizable. We can however approximate it by sampling the impulse response of the ideal continuous filter. The sampling rate must be at least twice the symbol rate of the message to transmit. That is, the filter must interpolate the data by at least a factor of two and often more to simplify the analog circuitry. In its simplest system configuration, a pulse shaping interpolator at the transmitter is associated with a simple down sampler at the receiver. The FIR structure with linear phase technique is efficient as it takes advantage of symmetrical coefficients and uses half the required multiplications and additions [8].

The rectangular pulse, by definition, meets criterion number one because it is zero at all points outside of the present pulse interval. It clearly cannot cause interference during the sampling time of other pulses. The trouble with the rectangular pulse, however, is that it has significant energy over a fairly large bandwidth. Due to this fact rectangular pulse is unsuitable for modern transmission systems. This is where pulse shaping filters come into play. If the rectangular pulse is not the best choice for band-limited data transmission, then what pulse shape will limit bandwidth, decay quickly, and provide zero crossings at the pulse sampling times? The raised cosine pulse is used to solve this problem in a wide variety of modern data transmission systems. This paper focuses on efficient design and implementation of WCDMA digital down convertor for software radios on an FPGA target device.

II. WCDMA DDC REQUIREMENTS

The DDC translates one or more intermediate IF channels from a set of specified centre frequencies to 0 Hz. It also performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR) [9]. For the reference design, the input to the DDC is a real signal sampled at 16xFchip = 61.44 MSPS and quantized to 14 bits. The complex baseband output are generated at a sampling rate of 2xFchip = 7.68 MSPS [10]. The WCDMA design parameters are shown in Table1. The DDC input is assumed to be real, directly coming from the ADC [11]. The mixer translates the real band pass input signal from intermediate frequency to a complex baseband signal cantered at 0 Hz [12].

Mathematically, the real input signal is multiplied by a complex exponential $e^{-j\omega_0 n} = \cos(\omega_0 n) - j\sin(\omega_0 n)$ to produce a complex output signal with real and imaginary components given by $Y_r(n) = X(n)\cos(\omega_0 n)$ and $Y_i(n) = -X(n)\sin(\omega_0 n)$, respectively. The sinusoidal waveforms required to perform the mixing process is obtained by using the Direct Digital Synthesizer (DDS).

There are several architectural options for the received signal path. The decimators in the DDC need to down sample the IF data from 61.44 MHz back to 2x chip rate. The factor of 61.44/7.68 = 8 can be partitioned using different possible configurations.

The down sampling by eight at once will result in an extremely long filter length and result in an inefficient hardware implementation [13, 14].

TABLE I
WCDMA DDC DESIGN SPECIFICATIONS

	Parameter	Value
1.	Carrier Bandwidth	5.0 MHz
2.	Number of Carriers	1 carrier
3.	IF Sample Rate	61.44 MCPS (16×3.84 MSPS)
4.	DDC Output Rate	7.68 MSPS (2xFchip)
5.	Input Signal Quantization	14-bit (Real)
6.	Output Signal Quantization	16-bit I and Q (Complex)
7.	Mixer Properties	Tunability: Variable Resolution: ~0.25 Hz SFDR: up to 115 dB

TABLE 2
FILTER CONFIGURATIONS

Anti-Aliasing Filter	**Filter Length & Sample Rate for 1st Filter**	**Filter Length & Sample Rate for 2nd Filter (if any)**
Configuration 1	31 taps (↓4) 61.44 MSPS	-
Configuration 2	11 taps (↓2) 61.44 MSPS	19 taps (↓2) 30.72 MSPS

Fig. 1 Hardware Efficient DDC

The use of shaping filter with decimation factor of 2 allows the remaining stages to be implemented as either one half band filter with decimation factor of 4 or two half band filters with decimation factor of 2 each. The two possible configurations of half band decimators are shown in Table2. The second configuration is more suitable for hardware implementation because of less hardware consumption whose block diagram has been shown in Fig1.

III. PROPOSED WCDMA DDC DESIGN

A hardware efficient Digital Down-Converter (DDC) is designed to meet the WCDMA specifications using a multistage half band decimator using Park McClellan algorithm based equiripple technique [15]. The first decimation filter is designed to reduce the sampling rate by 2. It is realized using the computationally efficient half-band filter structure, where every odd indexed coefficient is zero except for the centre tap and even indexed coefficients are symmetric [16]. The input sample rate of the filter is 61.44 MSPS, and the output sample rate is 30.72 MSPS, 8x the chip rate. The pass band was set to Fpass = 3.84*1.22/2 = 2.34 MHz and the pass band ripple is chosen to be 0.002 dB. It results in digital filter of order 10. The input and output precisions have been selected as 14 and 16 bits respectively to meet the WCDMA requirements. The 16 bit precision is used for coefficients quantization. The filter response is shown in Fig2 which exhibits stop band attenuation of 88.33 db.

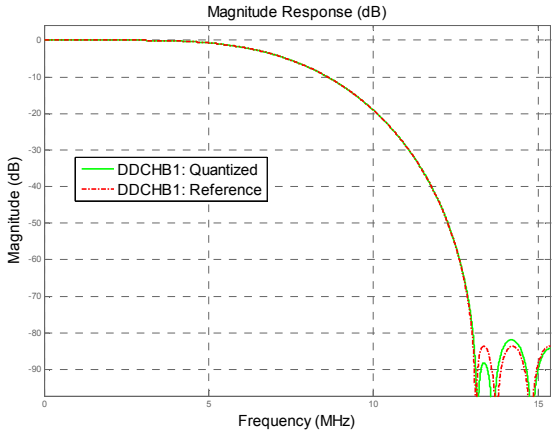

Fig 2. First Half Band Decimator Response

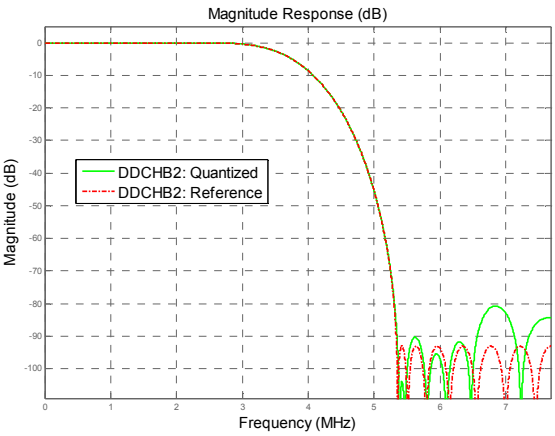

Fig 3. Second Half Band Decimator Response

The second half band filter further performs decimation by 2, from 30.72 MSPS to 15.76 MSPS. The pass band edge is set to 2.34 MHz and pass band ripple is set to 0.001 dB. It results in digital filter of order 26. The input and output precisions have been selected as 14 and 16 bits respectively. The coefficients are quantized using 16 bits. The filter response is shown in Fig3 which exhibits stop band attenuation of 102.84 db.

The next stage is RRC receiver channel filter. This filter also provides decimation by 2 to reduce the sampling rate from 15.36 MSPS to 7.68 MSPS, 2 times the chip rate. This 2x over-sampling rate is needed in the timing recovery process to avoid the signal loss due to the sampling point misalignment. The filter was designed with a cut off frequency of 1.92 MHz and a roll-off of 0.22 MHz. A Chebyshev window with 50 dB side lobe attenuation and filter order 60 has been used. The input and output precision of 14 and 16 bits are used along with 16 bit precision for coefficient quantization. The filter response is shown in Fig4 which exhibits stop band attenuation of 89.25 db.

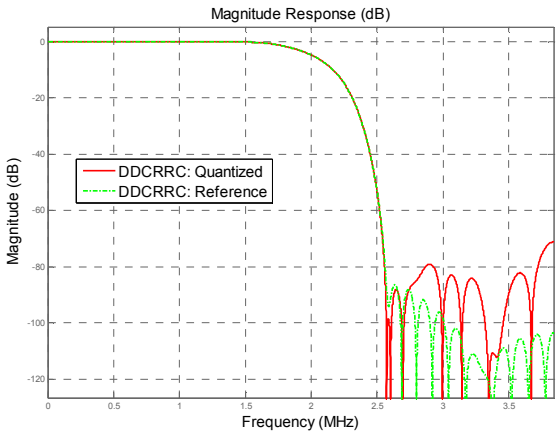

Fig 4. RRC Channel Filter

Finally all the three filters are cascaded to get final output response of WCDMA digital down converter which is shown in Fig 5.

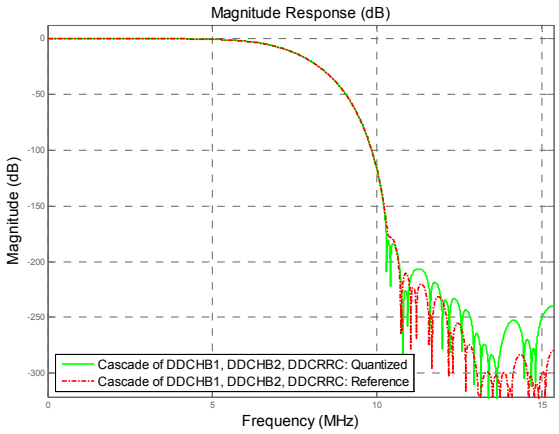

Fig 5. WCDMA DDC Response

IV. Hardware Implementation Results

The concept of polyphase decomposition and pipelined registers has been introduced to enhance the computational efficiency in implementing the proposed DDC. The proposed computationally efficient polyphase structure is shown in Fig6.

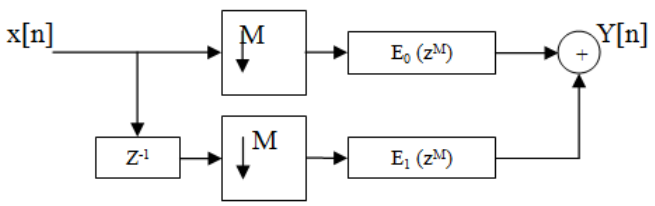

Fig 6. Computationally Efficient Poly Phase Structure

In this structure signal is decimated before filtering which reduces the number of coefficients required to implement the desired DDC. This coefficient reduction results in improved speed and power consumption of the proposed DDC design.

Then VHDL code is developed and synthesized on Virtex-II Pro based xc2vp30-7ff896 target device using Xilinx based Integrated Software Environment (ISE). The developed VHDL is simulated using ISE Simulator whose output response is shown in Fig 7.

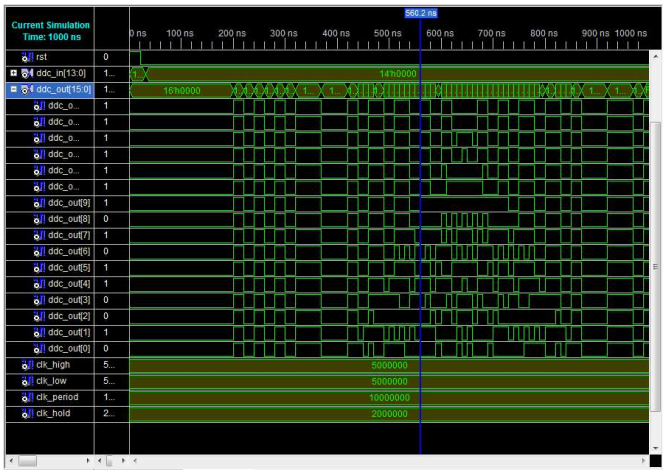

Fig 7. ISE Simulator Based DDC Response

The proposed DDC can operate at maximum frequency of 145.54 MHz as shown below:

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Timing Summary:
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Speed Grade: -7

   Minimum period: 6.871ns (Maximum Frequency: 145.545MHz)
   Minimum input arrival time before clock: 3.971ns
   Maximum output required time after clock: 3.293ns
   Maximum combinational path delay: No path found
```

The resource consumption of proposed design on specified target device is shown in Table3. The power consumption of the proposed DDC has been calculated using X Power Analyzer tool. The proposed design has consumed power of 0.10313W at 25°C junction temperature as shown in Table4.

TABLE 3
Resource Utilization

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1996	13696	14%
Number of Slice Flip Flops	3465	27392	12%
Number of 4 input LUTs	2267	27392	8%
Number of bonded IOBs	33	556	5%
Number of MULT18X18s	65	136	47%
Number of GCLKs	1	16	6%

The proposed WCDMA DDC is compared with existing design of [9] where System Generator based DSP48E blocks are used for implementation on Virtex-5 based XC5VSX50T FPGA device. The design implementation using in-built DSP48E blocks of System generator and target FPGA can

improve the time to market factor but cannot provide cost effective solution because FPGAs which contain DSP48E blocks are costly as compared to multiplier based FPGAs. In order to provide cost effective solution the proposed design has been implemented on Virtex-II Pro based xc2vp30-7ff896 target device which contains multipliers and is less costly as compared to Virtex-5 FPGA. The Park McClellan algorithm is proposed for optimal filter length to reduce the hardware requirement which is further supported by the concept of half band filter to improve the computational complexity for enhanced speed. Finally, Poly-phase decomposition technique is used in hardware implementation of proposed design to optimize both speed and area together by introducing the partially serial architecture.

TABLE 4
POWER CONSUMPTION

Name	Value	Used	Total Available
Clocks	0.00000 (W)	1	---
Logic	0.00000 (W)	2272	27392
Signals	0.00000 (W)	8231	---
IOs	0.00000 (W)	33	588
MULTs	0.00000 (W)	65	136
Total Quiescent Power	**0.10313 (W)**		
Total Dynamic Power	**0.00000 (W)**		
Total Power	**0.10313 (W)**		
Junction Temp	**25.0 (degrees C)**		

V. CONCLUSION

In this paper, an optimized hardware efficient technique is presented to implement WCDMA based digital down converter for software defined radios. The Park McClellan algorithm is proposed for optimal filter length to reduce the hardware requirement which is further supported by the concept of half band technique to improve the computational complexity for enhanced speed. Finally, Poly-phase decomposition based partially serial architecture is used in hardware implementation to optimize both speed and area together. The proposed WCDMA DDC is compared with existing design where System Generator based DSP48E blocks are used for implementation. The FPGAs with DSP48E blocks are costly as compared to multiplier based FPGAs. In order to overcome this problem the proposed design has been implemented on Virtex-II Pro based xc2vp30-7ff896 target device which contains in built multipliers. The proposed design can operate at maximum frequency of 145.54 MHz by consuming 0.10313W power at 25° C junction temperature. So the implementation of proposed DDC on specified target FPGA results in cost effective solution for software defined radios.

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