

A Low Power OTA for Biomedical Applications

N. Raj, R. K. Sharma, A. Jasuja and R. Garg

Abstract— New electronics for medical monitoring promise low-cost, maintenance-free, and lightweight devices which are critical in long-term medical measurements and in home-based tele-monitoring services. Operational Transconductance Amplifier (OTA) is a fundamental block of analog signal processing application particularly in Gm-C filter. A modified architecture of linearized subthreshold OTA for low-power, low-voltage, and low-frequency applications which incorporates better linearity and increased output impedance has been proposed in this paper. The OTA uses high output impedance low voltage current mirror to increase its impedance. The achieved open-loop DC gain is 71.49 dB at unity gain bandwidth (UGB) of 98.16 KHz. The OTA runs at power supply of 0.9 volt which makes OTA to consume power is 285.99 nanowatts. The circuit implementation has been done using standard 0.18 micron technology provided by TSMC on BSIM 3v3 level-53 model parameter and verified results through use of ELDO Simulator.

Index Terms— Bulk-input, OTA, Wilson mirror, UGB, Low voltage CM

I. INTRODUCTION

DEVICE sizing is the latest trend in VLSI. Scaling down the channel length in CMOS technology facilitates the submicrometer devices on single IC. Battery operated devices in medical electronics like Ambulatory Brain Computer Interface systems, insulin pumps; hearing aids essentially require low power designs using submicron devices. Such rapid increase use of battery-operated portable equipment is realized with VLSI (very large scale integrated) technologies. As the technology of biomedical instrumentation amplifier is moving towards portability; lower power consumption is highly desirable for devices which monitors patient whole day. Several methods had been proposed for reducing power consumption while retaining precision.

Biological signals like ECG is of small amplitude and low frequency range and to process these signals low pass filters with sufficient large time constant ($\tau = RC$) under an

acceptable capacitor value (typically less than 5 pf) is used. In general, low-pass filter with cut-off frequency less than 300 Hz is preferred for which continuous-time OTA-based filters are preferred [1]. However, major limitation of conventional OTAs is its limited linear range. A variety of linearization techniques have been proposed in which source-degeneration and multitanh [2] principle which improves linearity by eight to tenfold. As device sizes are scaling down, traditional saturation-based OTAs are facing design challenges to overcome poor linearity and limited output impedance. Recently, the bulk-driven technique has been applied in low-voltage analog building-blocks to deal with the problems caused by the limited scaled-down threshold voltage in the advanced technology [3]. Since, OTA is a voltage controlled current source (VCCS) device, it should have high output impedance. The proposed OTA in this paper provides a detail on ways to enhance output impedance using different architectures of Wilson mirror. The modified OTA maintains an appreciable linear range to handle loud sounds without distortion and enhance output impedance.

The proposed work has been organized into four sections. Section II covers the short review on bulk-driven MOS transistors. Section III describes a bulk-driven OTA and low-voltage CM circuit followed by proposed OTA. The simulation results and conclusion has been discussed in section IV and V respectively.

II. SHORT REVIEW ON BULK-DRIVEN MOS

Though the MOS transistor is a four-terminal device, it is most often used as a three-terminal device; a gate-driven transistor which is a strong function of threshold voltage. But threshold voltage of MOS transistors cannot be scaled down more than what are available today, creating difficulties for analog designers to design analog circuits with lower supply voltage. To accommodate low supply, bulk-driven MOS are preferred over gate-driven MOS. In gate-driven MOS transistor, the gate-to-source voltage controls the drain current of the transistor while for a bulk-driven MOS transistor where threshold voltage is a function of the bulk-to-source voltage; controls the drain current. When using a single MOS transistor as an amplifier, the input signal is usually fed into the gate terminal whereas the bulk-terminal is tied to fixed bias (V_{ss} for NMOS and V_{dd} for PMOS). For a bulk-driven MOS transistor, the input signal is fed into the bulk whereas gate-terminal is fixed to constant supply. The operational characteristics of the bulk-

Manuscript received December 12, 2010.

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driven and gate-driven NMOS transistors are illustrated in Fig. 1.

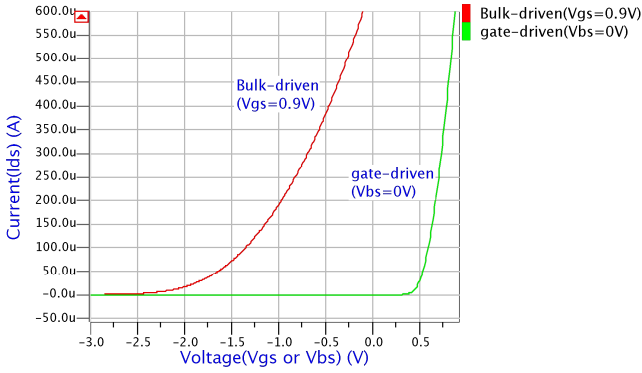


Figure1 Comparison of Ids Vs Vgs (or Vbs)

It can be observed that the gate-driven NMOS transistor in active region requires atleast the threshold voltage drop (approx 0.375 volts). On the other hand, bulk-driven NMOS transistor behaves like depletion NMOS transistor; that is, with zero-input bias voltage at bulk-terminal the transistor will remain in active region [4]. Such advantage encourages the use of bulk-input transistors for designing of low-supply voltage analog circuits. Besides advantage of bulk-input MOS, it faces some disadvantage detailed in [5]. The main drawback is its low open-loop gain (as g_{mb} is less than g_m value). Secondly, the polarity of bulk-input MOS is process related as wells are required to isolate the bulk-terminals. So, in standard digital CMOS technology (n-well process) only PMOS can be used as bulk-driven otherwise if both polarities need to be bulk-driven then a twin-well technology will be required.

III. PROPOSED SCHEMATICS

A. The Cited OTA

OTA is a key functional block used in many analog and mixed-mode circuits, and subthreshold operation is a natural choice for low-power, low-voltage, and low-frequency applications. The ideal OTA has infinite bandwidth and infinite input and output impedance whereas all other nodes have low impedance.

The main drawback in conventional OTA as already discussed is its limited linearity and low output impedance. Various techniques had been employed to overcome poor linearity of gate-driven OTA but an appreciable amount of linearity has been achieved in bulk-driven OTA. The core bulk-driven OTA [6] referred in this paper is shown in Fig. 2. It provides a linear range of about 1.7 volt. The OTA uses well terminals of the differential-pair transistors W_1 and W_2 as inputs. The negative feedback, that is, source degeneration via S_1 and S_2 transistors whereas gate degeneration via GM_1 and GM_2 provide further

improvement. The bump transistors B_1 and B_2 overcome parasitic effects. The rest of transistor is configured as current mirror whereas transistor P provides bias current I_{bias} to OTA. The output equation is given by

$$I_{OUT} = I_B \tanh\left(\frac{V_d}{V_L}\right) \quad (1)$$

where, V_d is differential input voltage and V_L corresponds to linear range given by $V_L = 2V_T/g$. Here, g is the overall transconductance of OTA which is decreased by the loop gain of negative feedback in order to enhance linearity.

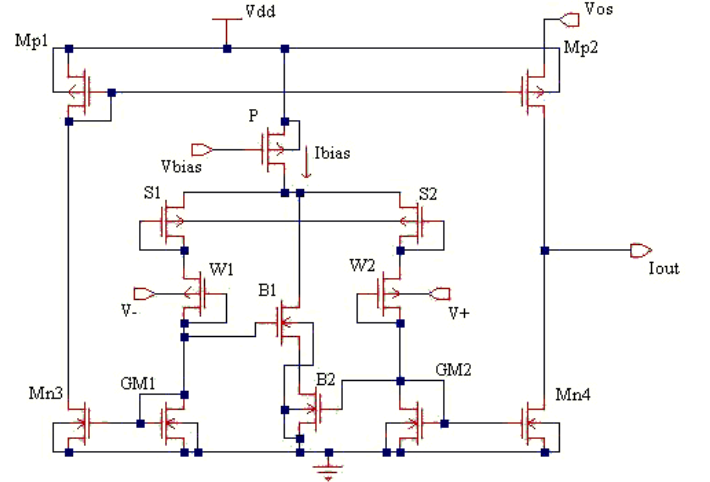


Figure 2 Cited OTA [6]

The main drawback of this OTA lies in its offset voltage adjustment V_{os} (few mV less than V_{dd}) due to parasitic effect which appears at low input voltage of less than one volt when configured as follower integrator at 1pf of capacitive load. To overcome such offset and improvement in linearity has been achieved using various techniques. The proposed work is focused on to achieve high output resistance and increased open-loop DC gain at the cost of low UGB. The proposed OTA uses High output impedance low voltage current mirror as a replacement to earlier mirroring techniques described in [7].

B. High Output Impedance low voltage CM

A current mirror is characterized by the current level it produces, the small-signal ac output resistance and voltage drop across it. Simple CM provides small output resistance which has been increased through use of various Wilson topologies. The key factor of using Wilson mirror is that besides mirroring it provides negative feedback which stabilizes the fluctuations occurring at output. The Wilson architecture preferred for OTA design in [7] is shown in Fig. 3. As seen from architecture of Fig. 3, it sense the output current at low input voltage of a diode drop plus a saturation voltage whereas output senses only two saturation voltage. The diode connected transistor on input side biased by current source I_b causes the input voltage to decrease

much lower than gate voltage needed as in case of simple current mirrors to sink input current. This makes it a low voltage high-swing CM circuit.

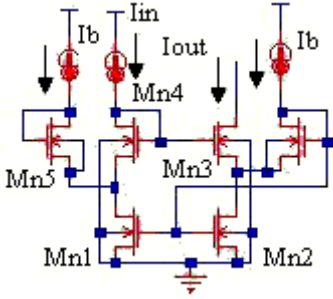


Figure 3 High-swing improved Wilson CM [8]

The mirror achieves high output resistance by using negative feedback and is directly proportional to the magnitude of the loop-gain of the feedback action from the output current to the gate of output transistor M_{n3} . The small-signal output resistance (neglecting 2nd order effects) is given by

$$r_{out} = r_{o3} \left(1 + \frac{g_{m3}(1 + g_{m1}r_{o1}) + g_{o3}}{g_{m2} + g_{o2}} \right) \approx g_{m1}r_{o1}r_{o3} \quad (2)$$

The transistor M_{n4} forces the drain voltages of M_{n1} and M_{n2} to be equal and reduces unwanted offset in the output current.

The transistor M_{n4} exhibits low output resistance of $1/g_{m1}$. In order to enhance its output resistance, the diode

structure is replaced by cascode one as shown in Fig. 4. The mirror provides an increase in output resistance [9] by a factor of $g_{m4}r_{o4}$. Thus, output resistance equation results as

$$r_{out} = r_{o3} \left(1 + \frac{g_{m3}(1 + g_{m1}g_{m4}r_{o1}r_{o4}) + g_{o3}}{g_{m2} + g_{o2}} \right) \approx g_{m1}g_{m4}r_{o1}r_{o3}r_{o4} \quad (3)$$

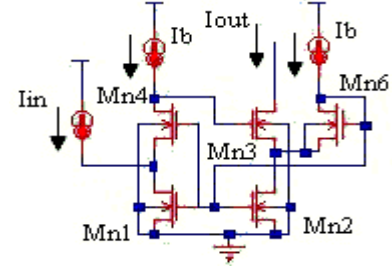


Figure 4 High output impedance low-voltage CM [9]

C. Proposed OTA

The proposed OTA using High output impedance low-voltage CM is shown in Fig. 5. The circuit works on low supply voltage thereby introducing appreciable reduction in power consumption. A bias current generator generates current in range of nano amperes configured to the OTA for I_{bias} . The current generator circuit consists of transistors $M_{n13} - M_{n16}$ and $M_{p11} - M_{p12}$ along with R_s . Using the saturation current equation (neglect channel length modulation) and solving for gate-to-source voltage, the required bias current equation is obtained.

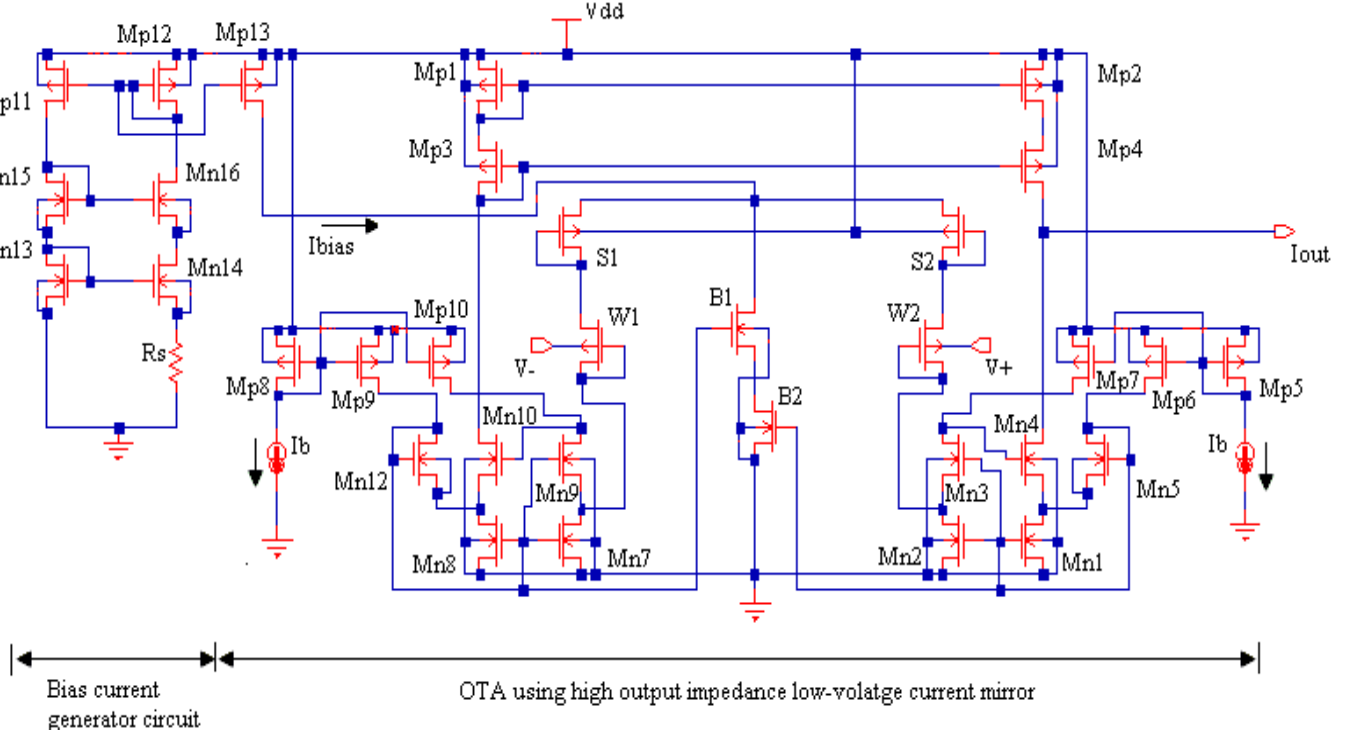


Figure 5 Proposed OTA using High output impedance low-voltage CM

From left-half circuit, it can be observed that

$$V_{GS,n13} = V_{GS,n14} + I_{D,n14}R_S \quad (4)$$

Solving for V_{GS} and equating equivalent currents

$$\sqrt{\frac{2I_{D,n13}}{\mu_n C_{ox} (W/L)_{M_{n13}}}} = \sqrt{\frac{2I_{D,n14}}{\mu_n C_{ox} (W/L)_{M_{n14}}}} + I_{D,n14}R_S \quad (5)$$

The final expression for I_{bias} is given as

$$I_{bias} = I_{D,p12} = \frac{2}{\mu_n C_{ox} (W/L)_{M_{n13}}} \frac{1}{R_S^2} \left(1 - \sqrt{\frac{(W/L)_{M_{n13}}}{(W/L)_{M_{n14}}} \right)^2 \quad (6)$$

By adjusting the (W/L) ratio of M_{p13} relative to M_{p12} ; desired I_{bias} can be obtained. The remaining right-half circuit comprises of referred basic OTA employed with High output impedance low-voltage CM.

IV. SIMULATION RESULTS

The proposed OTA performance is compared to the architecture discussed in [7]. The simulations were performed under normal condition (room temperature) on TSMC 0.18 micron technology using ELDO Spice Simulator. The bias current generator circuit generates I_{bias} of 65nA at $R_S = 10K\Omega$. The supply voltage has been kept at 0.9 volt. Fig. 6 shows the transfer characteristics (linear range) of proposed OTA which shows linearity near about ± 1.9 volt with no offset voltage adjustment.

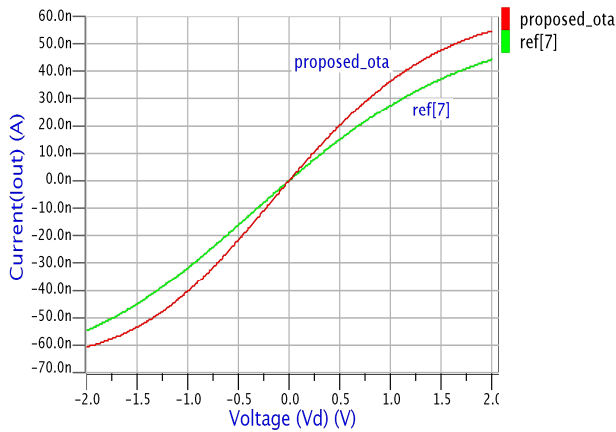


Figure 6 Transfer characteristic (Linear range) of proposed OTA

Fig. 7 shows the ac response of proposed OTA under no load condition. The achieved open-loop DC gain and UGB of proposed OTA is 71.49 dB and 98.16 KHz respectively. Its low UGB supports it for use in biomedical applications.

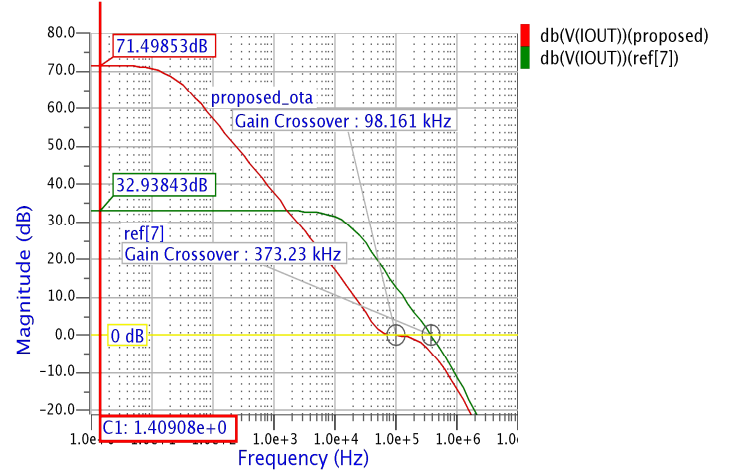


Figure 7 AC response showing DC gain and UGB of proposed OTA

When configured as follower integrator using 1 pf of load shown in Fig. 8; it tracks the input with almost no parasitic effect even at low input voltage. The dc response of follower integrator is shown in Fig. 9.

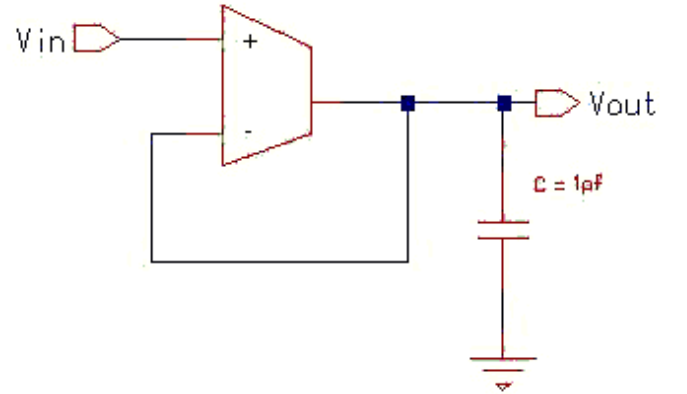


Figure 8 Follower integrator

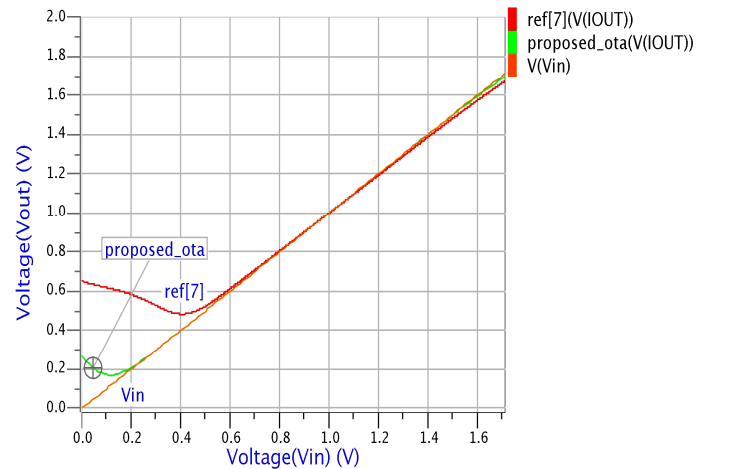


Figure 9 DC response of follower integrator of proposed OTA

ACKNOWLEDGMENT

The total power consumption of proposed OTA is 285.99 nanowatts shown in Fig. 10.



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Simulating design : wilson_improved_edit/tsmc018a

SIMULATION INFORMATION
memory size allocated in bytes 5595319
nb of components: 135
nb of nodes: 123
nb of MOS or BIP calls: 411767
Number of steps computed: 0

***>CPU TIME 2s 700ms <***

Performing DC analysis...
--> Partitioning circuit...

***> DC CPU TIME 0s 020ms <***

DC:20 iterations FOR DC analysis

TOTAL POWER DISSIPATION: 285.9905N WATTS
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Figure 10 Total power consumption of proposed OTA

V. CONCLUSION

The proposed work explores the approach of low-voltage OTA design using the bulk-driven technique and enhancement of output impedance achieved using high output impedance low-voltage CM circuit. With the help of the integrated circuit technology, medical diagnostic instruments can be compacted to portable devices for the purpose of homecare to diagnose heart disease. The design of such low voltage, low UGB OTA satisfies the required parameters for its implementation not only in power-saving devices but also in biomedical portable devices for reducing health-care costs. Further it can find application in variable gain amplifiers, oscillators, balanced resistive bridges and analog filters.

The authors would like to thank R. Sarpeshkar, R. F. Lyon, and C. A. Mead for meaningful discussions on bulk-input OTA and also to B. A. Minch, and L. F. Tanguay for the measurement assistance of different CM circuits. The authors extend their thanks to generous support of VLSI Design Lab of ECE department at NIT Kurukshetra and financial assistance given by Special Manpower Development Programme (SMDP) project sponsored by ministry of communication and information technology, government of India.

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