Design and Implementation of A CMOS Tunable Phase Shifter

A. Mohammadi, A. Ayatollahi, and A. Abrishamifar

Abstract— **A tunable phase shifter for high frequency applications is proposed. The idea is inspired from the current mirror operation principle. Exploiting the current mode approach extends the operation frequency of the phase-shifter up to the transistor cut-off frequency. The performance of the proposed circuit was verified via experimental results at low frequencies with the available off-the-shelf components. The prototype was implemented by CMOS (Complementary Metal Oxide Semiconductor) gates on a chip (CD4002). The simulated power consumption of the circuit implemented in 0.18um TSMC CMOS technology is 80 microwatts which covers a wide frequency range. The elimination of inductor, loss-less input-output characteristic and accurate phase change are the notable features of the circuit addressed in this work.**

Index Terms—**Phase shifter, CMOS, Current mode**

I. Introduction

PHASE-shifters have found numerous applications including digital communication systems, in which a clock has to be optimally adjusted with respect to the data stream, instrumentation [1], pulse generators, etc. They have also been used in delta-sigma analog to digital converters to linearize the inherent nonlinearity of voltage controlled oscillators [2]. For these applications, the phase of the arbitrarily shaped clock signals should be continuously adjustable in a simple manner [3]. Phased array subsystems, which are widely used in wireless communication, also utilize the phase shifters. Their two main applications in this field are in radars and high data rate communications [4, 5].

Integration of a complete phased array system in silicon leads to substantial improvements in cost, size, and reliability [6]. At the same time, it provides numerous opportunities to perform on-chip signal processing and conditioning, without having to move off the chip, leading to additional savings in cost and power.

The phase shift necessary in each element of a phased array can be achieved at RF (Radio Frequency), at base-band/IF (Intermediate Frequencies), or in the LO (Local Oscillator) path [5]. Phase shifting at RF path is preferred in comparison with IF or LO path because the RF output signal has high pattern directivity. In terms of telecommunication systems, it can substantially reject interferers before a RF mixer, relaxing the mixer linearity and overall dynamic range requirement [7]. However, it has design issues associated with high frequency circuits. There are several methods to implement phase shifters including switched line and variable reactance reflection phase shifter. Inductors are commonly used in high frequency phase-shifter architectures (passive or active) in order to realize the all-pass transfer function. In addition to complex integrated circuit fabrication process, this increases the footprint of the phase shifter. Also the low quality factor of integrated inductors have adverse effects in the phase shifter performance [8]. The only architecture that reports a reflection type CMOS phase shifter uses the active inductors [9].

In the following section the basic design idea for the new radio frequency phase shifter is discussed. Subsequently, the design procedure is explained in section III and simulation results are demonstrated. Finally, the measured results are shown to prove the performance of the proposed circuit.

II. Realization of All-pass transfer function

According to [10] the basic passive circuit for realization of the all-pass transfer function, in voltage mode, is sketched in Fig. 1. The procedure by which the all-pass transfer function is realized is of particular interest here.

At the positive output node (Vo^+), a constant ratio of the input voltage is generated and at the negative one (Vo^-), the input voltage is fed through a low-pass filter. The output is as

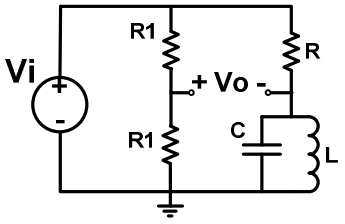

Fig. 1. Basic voltage-mode realization of passive all-pass filter

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follows:

$$Vo = \frac{1}{2}Vi - \frac{\frac{s}{RC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}}Vi$$

$$\frac{Vo}{Vi} = \frac{1}{2}\frac{s^2 - \frac{s}{RC} + \frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \qquad (1)$$

Equation 1 is a second order all-pass transfer function which is produced by subtracting the low-pass term from the constant ratio. The zeros and poles of such a system are complex conjugates.

The active circuits are preferred to the lossy passive ones while at the receiver the input signal power is low. In addition the passive implementation of the phase shifter needs the inductors which are not easy to integrate in the CMOS planar technologies. Also the phase-shifter is located in the front-end of the receiver; then, its noise dominates the system noise figure. Commonly fewer number of devices leads to lower noise level [11]; consequently, the simplicity of the design is demanding.

In this work we have implemented the all-pass transfer function by applying the aforementioned idea to a current signal, i.e. input current signal is subtracted from its low-passed counterpart to generate an all-pass transfer function. The obtained transfer function provides the phase shift for the input signal. In the following section, the circuit design steps are explained in more detail.

III. Basic Circuit for the Proposed Phase Shifter

The implementation procedure for the proposed topology is inspired from the inherent gate-drain capacitance of metal oxide semiconductor (MOS) transistor, C_{gd}. Because of its smaller size, in comparison with gate-source capacitance (C_{gs}), this capacitor appears at higher frequencies. As shown in Fig. 2 the input current signal passes through two different paths to reach to the output. The direct path is through C_{gd} and the other one is through g_m in which the current signal undergoes a 180˚ phase shift. These are shown by the path 1 and 2 in Fig. 2, which is a rough high frequency model of MOS transistor. So according to the operating frequency and the transistor bias, which determines the frequency response of the transistor, different combinations of these two signals would flow at the output.

In order to handle the input received signal from antenna and controlling the MOS bias, the current mirror topology is proposed in this work, as illustrated in Fig. 3. Mb is used to provide bias current of the circuit. Only its drain capacitance is effective on the frequency response by adding to the gate and drain capacitance of M1. Here, the design idea follows the simple realization of the all-pass transfer function in Fig. 1, except the current signal is handled instead of voltage signal in (1). Accordingly, a constant ratio of input current signal (*Ii*) would be subtracted from its low-passed counterpart. *Ii* is the input ac current signal received form the low noise amplifier and *Io* is the ac current signal output to the following stage which is often a mixer [7].

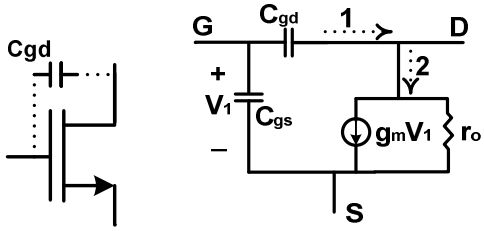

Fig. 2. MOS Model and Paths 1, 2 for Output Signal

C_c is a coupling capacitor which is placed only for dc isolation of load R_L which is assumed to be 50 ohms to be matched to the following stage.

The current transfer function would be extracted via the equivalent circuit in Fig. 4 as follows. Also it should be noted that to extract the current transfer function, the output is short circuited; the same as it is for extracting the h_{21} parameter of hybrid transfer functions [12]. Furthermore the drain-source resistance of MOS transistors (r_{DS}) in the equivalent circuit is ignored since in case of M1 as a result of the drain-gate short circuit, r_{DS} acts the same as g_{m1} and consequently, it's negligible. In case of M2, the output of circuit is short circuited to obtain the current transfer function, thus avoids r_{DS2} to pass any current.

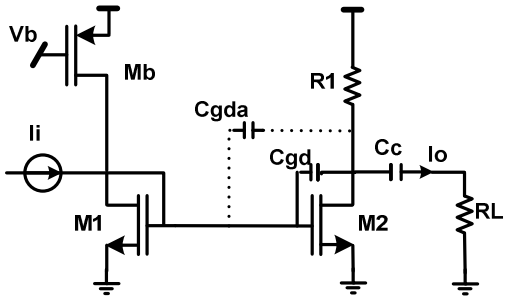

Fig. 3. Proposed Current Mirror Phase Shifter (C_{gda} is added between gate and drain to increase C_{gd})

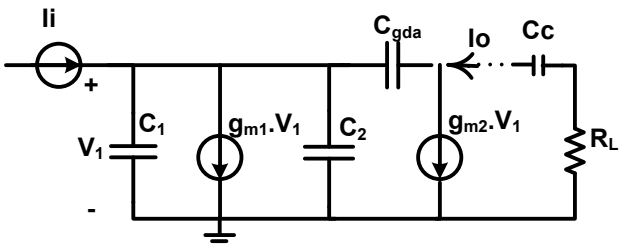

Fig. 4. Equivalent circuit of proposed phase shifter

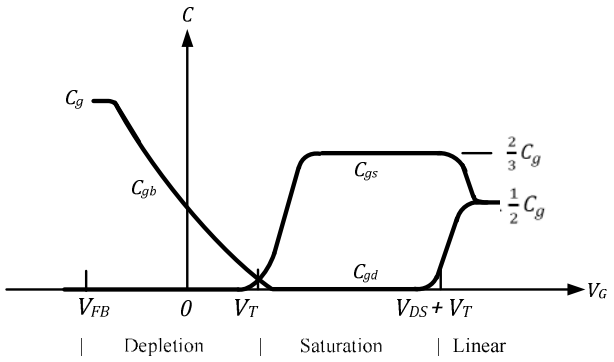

Fig. 5. MOS capacitances based on region of operation

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$$Ii + Io = ((C_1 + C_2)S + gm_1 + gm_2) \times V_1 \quad (2)$$

$$V_1 = \frac{Ii}{(C_1 + C_2 + C_{gd})S + g_{m1}} \quad (3)$$

$$\frac{Io}{Ii} = \frac{C_{gd}}{C_1 + C_2 + C_{gd}} \times \frac{S - \frac{g_{m2}}{C_{gd}}}{S + \frac{g_{m1}}{C_1 + C_2 + C_{gd}}} \quad (4)$$

$$[C_1 = C_{gs1} + C_d(Mb), \quad C_2 = C_{gs2}]$$

Comparing (4) with a first order all-pass transfer function (5), in which A is its magnitude and α is the location of pole and zero, the following relation between circuit parameters would be obtained as a necessity.

$$T_{all-pass} = A\frac{S - \alpha}{S + \alpha} \quad (5)$$

$$C_{gd} = \frac{g_{m2}(C_1 + C_2)}{g_{m1} - g_{m2}} \quad (6)$$

From (6) it is inferred that transconductance of M1, g_{m1}, should be larger than g_{m2} for C_{gd} to be realizable.

Capacitor C_{gd} is also a nonlinear voltage dependent oxide capacitor [13] which is so smaller than C_{gs}. According to Fig. 5 the only way to increase the C_{gd} is to drive the transistor in the triode region which is not reliable for the current mirroring function. However, a more convenient way is to add an extra capacitor between the gate and drain (C_{gda}) as shown in Fig. 3. Due to the minimum feature of CMOS transistor technology file that is used in our simulation (0.18um), the transistor capacitances are in the range of femto farads (fF). Therefore, to avoid the gate-drain capacitance vary as a function of the output voltage we have chosen the nominal value of the adjunct capacitor (C_{gda}) to be an order of magnitude larger (10fF). As a result the current magnitude would not attenuate much. From this point on we will use C_{gda} instead of C_{gd} + C_{gda}.

From equation (4) and assuming the parasitic to be negligible (unless they might increase the system order), the phase relationship for the current transfer function is obtained through (7).

$$\Phi(\frac{Io}{Ii}) = -2\tan^{-1}(\frac{\omega}{\alpha}) = -2\tan^{-1}(\frac{C_{gda}}{g_{m2}}\omega) \quad (7)$$

This relationship implies that to achieve different phases in a fixed frequency both C_{gda} and g_{m2} could be altered. However, the magnitude of the transfer function must be kept fixed at different phases. As illustrated in (4), (5) the magnitude of current transfer function (A) is affected by C_{gd} and C_1+C_2. So if we choose the sweeping range of C_{gda} much larger than C_1+C_2, then A will be close to unity and approximately independent of C_1+C_2.

On the other hand altering the C_{gd} would change the symmetric location of pole and zero of the system and consequently the all-pass behavior wouldn't be preserved. So to further control the phase shift we must alter the transconductance (g_m) of the transistor.

Variable transconductance might be achieved by either altering the aspect ratio or the bias currents of M1, M2. The former changes the internal capacitors of transistors and falsifies the initial assumptions. Though, the latter, can achieve fine tune while preserving the all-pass behavior. Consequently, a tradeoff between the achievable phase tuning range and minimum gain (A) error (caused by choosing Cgda to be much larger than C1+C2) exists.

A. Coarse tune and fine tune

As mentioned before by switching between the C_{gda} capacitances, different phase shifts are obtainable. In order to control the amount of phase change continuously and with high precision, we utilized MOS varactors in parallel with the

previously discussed switch-able large capacitors. This technique is almost often exploited in voltage controlled oscillators to achieve coarse/fine tune of the output frequency [13].

MOS varactor might be a PMOS or an NMOS transistor whose drain and source are connected to each other as one terminal and the gate as the other terminal of the capacitor, as illustrated in Fig. 6. In order to control the capacitance the next topology is used where the control voltage is applied to the common gate as shown in Fig 6.b. Consequently the fine control could be achieved through an independent input.

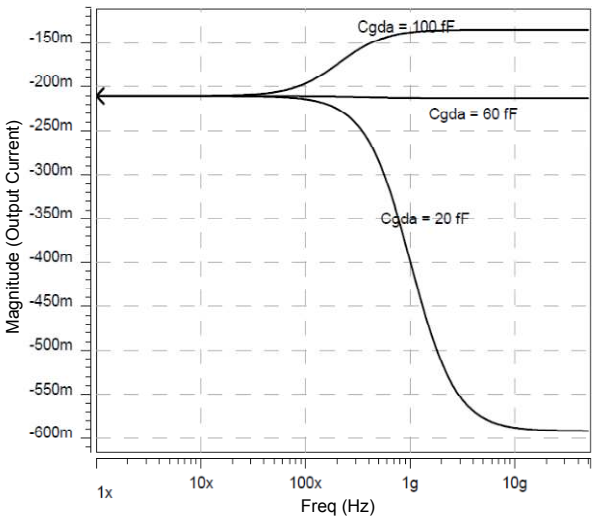
The available models for the standard CMOS processes are incapable to determine the required area to generate a definite amount of capacitance and the only way is to rely on simulation tools in design step. However, the proposed fine control is able to mitigate the inconsistencies of the fabrication process.

IV. Simulation Results

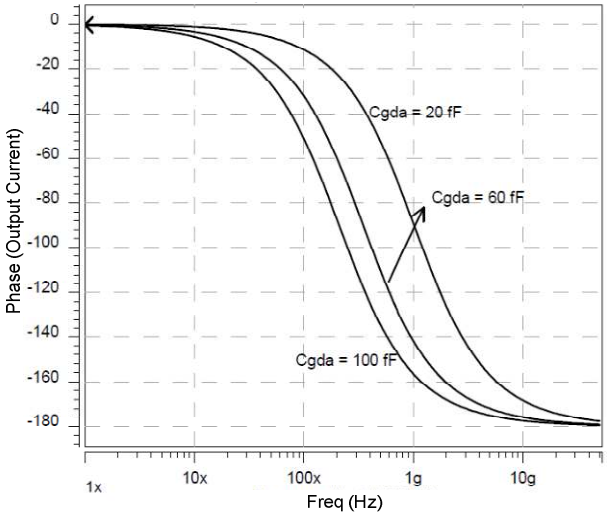
The 0.18um CMOS (complementary metal oxide semiconductor) technology file is utilized in our Hspice simulation. The supply voltage is 1.8v. As shown in Fig. 3, a unity ac current is supplied in to the phase shifter (Ii), and the output current (Io) is read out. The load resistor is 50ohm to be matched with following stages and coupling capacitor is large enough to avoid its effect on phase shifter performance.

As explained in the previous section the first approximation for C_{gd} is done to be in the order of 10fF. So, the simulation has been carried out by sweeping C_{gd} for 20fF, 60fF, 100fF. As illustrated in Fig. 7 the second iteration (C_{gd}=60fF) makes the least current perturbation.

Obviously, the all-pass characteristic is achieved only for one the capacitors (C_{gd}=60fF). Therefore, in order to keep the amplitude of the output signal constant, while changing its phase at a given frequency (phase shifter function), simultaneous C_{gd} and transcondactance variation is required. Consequently, the transconductance of the mirror transistors



(a)



(b)

Fig. 7. Simulated output current a) magnitude and b) phase.

are manipulated by varying their bias current. Accordingly, the gate voltage of Mb in Fig. 3 is swept for 0.5v, 0.75v and 1v as illustrated in Table 1. This was kept fixed at 0.75v in the previous step.

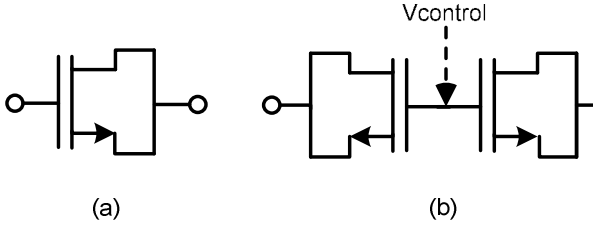


Fig. 6. Cgd implementation by a) MOS varactor b) MOS varactor with control input

TABLE I
Output Current Phase

Frequency (Vb)	0.1GHz (0.5v)	1GHz (0.75v)	10GHz (1v)
Amplitude	-0.2dB	-0.2dB	-0.2dB
Phase(Cgd=60fF)	-32˚	-142˚	-176˚
Phase(Cgd=100fF)	-52˚	-155˚	-178˚

V. Implementation and Measurement Results

Since our main idea is not very frequency dependent, therefore for the sake of simplicity to verify our idea we implemented the proposed circuit on CD4007 which operates on lower frequencies [14]. It consists of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals. Some ports of these transistors are connected together internally, in a

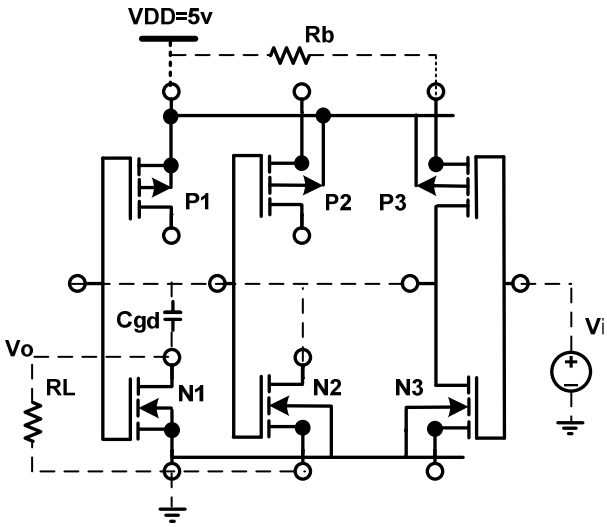


Fig. 8. Implemented phase shifter on CD4007: solid lines and dashed lines are internal and external connections, respectively.

way that not all of them are usable independently. The way that we have connected them is shown in the figure 8. Solid lines are internal connections and dashed lines are the external ones we added to achieve the desired topology. N1, N2 and P3 are involved respectively as M2, M1, and Mb in figure 3. Voltages on Rb and RL are in phase with their currents. Vi is the small signal input plus the bias voltage of P3.

Almost all available signal generators are of the voltage type rather than current type. Here we have applied the input voltage signal to the gate of Mb in figure 3, as well as the bias voltage. Then a current signal would be generated at the drain of Mb and fed into current mirror.

As illustrated in figure 9.a, the input and output signals are measured after changing the C_{gd} by 100pf steps. The first inset for C_{gd}=0 which shows a 3.432˚ phase difference. Then for each 100pf step, phase shift of about 7˚ happens while the output signal is not constant. This would be mitigated if we change the transconductance of M1, M2 as mentioned before. Final results are shown in figure 9.b, where the simultaneous transconductance variation as well as C_{gd} demonstrates constant amplitude (1.120Vp-p) for different phase shifts. The transconductance variation is

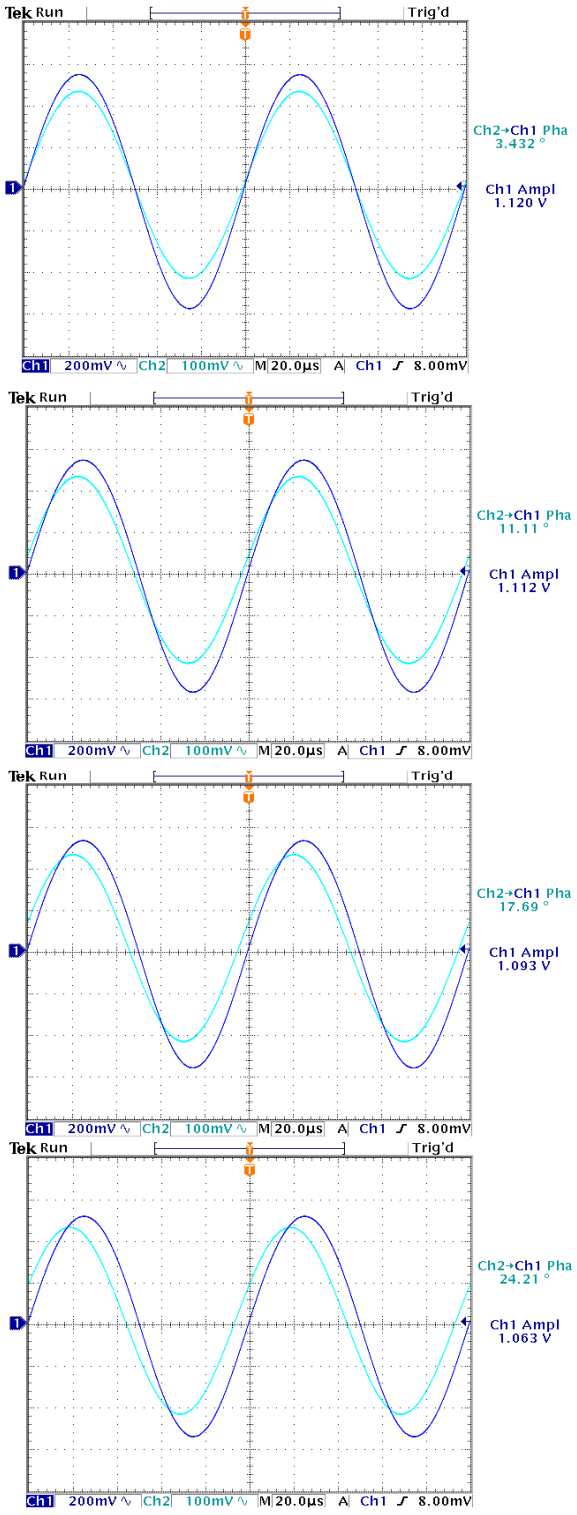


Fig. 9.a : Phase shifted signal for Cgd 100pf steps

achieved by varying the Mb (P3) bias voltage. The first inset is not repeated in figure 9.b.

Also the power consumption of circuit is 80 microwatts from 1.8v dc supply, which is reasonable for low power applications such as handheld systems.

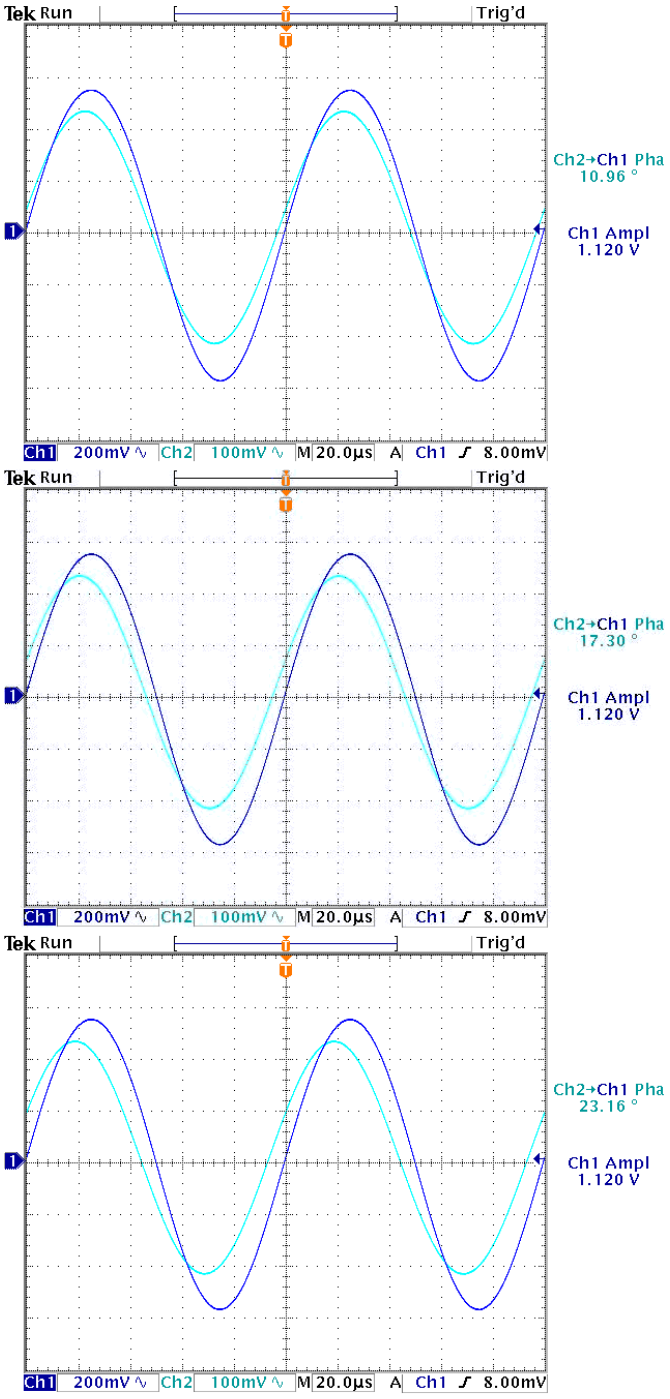


Fig. 10.b : Constant amplitude (1.120v) phase shifted outputs

VI. 6 Conclusion

The proposed technique, utilizing the current mode approach provides continuous phase shifts in a wide frequency range as illustrated in Table 1. Also it's possible to switch between different capacitances to have different phase shifts in a specific frequency. Different transconductances for transistors should be selected to preserve the all-pass characteristics. The frequency band desired for a phase shift to take place is determined primarily by C_{gd}. As higher frequency as wanted, the C_{gd} must be smaller and that will be limited by parasitic capacitances. The simulation results are compared with similar works in Table 2. Lower loss and power consumption are prominent characteristics of the proposed circuit. Since the minimum feature is used in this work to offer higher frequency response the area is expected to be smaller than similar works. The operation of the circuit follows the same scenario at lower frequencies; hence, we utilized the available off-the-shelf integrated circuit CD4007 to approve the design.

TABLE 2: Comparison with other works

Reference	Technology	Phase shift	Loss	Frequency Band	power
[9]	0.18um CMOS	90°	1.5 dB	2.3~2.5 GHz	12mW
[8]	0.18um CMOS	22.5°	2 dB	2~10 GHz	na
This work	0.18um CMOS	13°	0.2 dB	1-10 GHz	<1mW

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