A Low-Power Multiphase-Delay-Locked-Loop with a Self- Biased Charge Pump and Wide-Range Linear Delay Element

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***Abstract*— A low power Multiphase-Delay-Locked-Loop (MDLL) with a self-biased Charge Pump (CP) and a wide-range linear delay element is presented. Body feed technique and proper voltage converters are utilized in the proposed Voltage-Controlled-Delay-Line (VCDL) to widen applicable range of control voltage and overcome the nonlinearity of the conventional current starved delay element. Moreover, improving the noise performance is achieved by taking advantage of the differential structure. A new self-biased CP with a control circuit is proposed to suppress mismatch problem in single ended CPs. The designed circuit has been simulated in ADS software, using TSMC-CM018RF-PROCESS with a 1.2V supply voltage. The operating frequency range of the proposed MDLL is from 185 to 650 MHz. The maximum and minimum rms jitters are 20 and 1.5 ps, respectively. The maximum power dissipation of the designed circuit at 650 MHz is 1.1 mW.**

***Index Terms*— Delay element, charge pump, delay locked loop, bias circuit.**

I. NTRODUCTION

IN recent years, DLL has attracted great attention for integrated circuits [1]. In multi-phase clock generators, such as timing recovery [2], BIST circuit [3], and frequency multiplier [4], the circuit function is implemented by the multiphase-output of the VCDL in DLLs. Fig. 1 shows a typical building block of a conventional analog MDLL, which consists of a VCDL, a Phase-Frequency-Detector (PFD), a charge pump (CP), a loop filter (LF). A reference clock progresses through the VCDL. The PFD encloses the VCDL and constantly monitors the phase error between the reference clock at the beginning and the end of the line, and continuously transfers the error information to the CP, which converts the phase error into current, pumped into the LF to generate the control voltage (Vc), and thereby adjusts the VCDL delay. Due to such a negative feedback mechanism, the phase error is gradually reduced until it finally approaches zero, which indicates that the loop has been locked.

In analog DLLs, the delay range of the VCDL will directly limit the operating range of the circuit [5]. A serious problem with conventional VCDL structure is that the variation of output propagation delay is not linearly related to the control voltage. A nonlinear delay variation greatly reduces the quality of the VCDL performance. When the control voltage is nearby the threshold voltage, the delay is very sensitive to variations in the control voltage and noise [6].

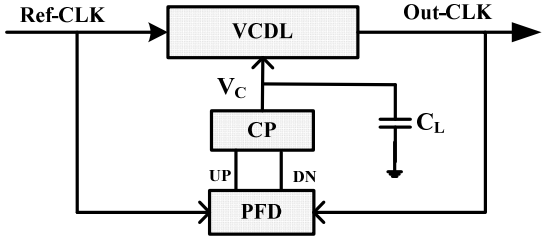

Fig. 1. Conventional analog MDLL.

Moreover, the PFD and the CP are also critical components within a DLL. Ideal PFD/CP should provide an infinite DC gain for any phase difference at the inputs of the PFD. Ideally both the "UP" and "DOWN" signals should not be high at the same time, which leads to a dead-band region. In principle, the CP consists of two controlled switches, one current source (Iup), and one current sink (Idn), where the switches are controlled by the "UP" and "DOWN" pulses. The CP adds/ subtracts charge to/from the loop filter (CL) [3]. Because of mismatch problem in CP, any width of the dead-band region directly translates to jitter in the DLL [5].

In order to suppress this problem, the charge pump must transfer no net charge to the loop filter for these equal duration, so "UP" and "DOWN" currents should be identical and independent of the charge pump output voltage. By using additional techniques like feedback circuits, replica CP's, or additional compensation CP's, better performance can be achieved but at the expense of the CP simplicity [8]-[10]. Even if Iup and Idn are identical, the switching time difference between the controlling signals applied to the PMOS and NMOS switches will cause the voltage variation of

Manuscript received April 10, 2011. This work was supported by the Iran Communication Research Center.

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the loop filter and increases the output jitter in the DLL.

In the proposed MDLL the *"UP"* and *"DOWN"* output pulses of PFD are produced at each cycle to eliminate dead-band problem; whereas, by using a control circuit at the input of *"UP"* and *"DOWN"* switches, output currents of CP cannot flow simultaneously. In this way, the mismatch problem is extinct in single ended CPs. To improve the linearity of VCDL and allow rail-to-rail operation for the delay control voltage, the body feed technique with proper bias generators are employed. The rest of this paper is organized as follows. Section II explicates the architecture of the proposed MDLL. The simulation results are shown in Section III, and conclusions are given in Section IV. Proposed MDLL Circuit

The simple loop characteristics belie many subtleties in DLL design [4]. Low power, wide lock range, short locking time, and low jitter are the focuses of the DLL design. In order to achieve low jitter operation, DLL designs require delay stage design with low supply and substrate noise sensitivity [11] and good matching between the up/down CP currents. To realize the high-frequency MDLL, the accuracy of the PFD and the bandwidth requirement of the delay cells in the VCDL should be considered. In many cases to achieve these features some additional circuits are utilized in DLL loop that increase the power consumption and complexity of the circuit. In this work, the proposed analog-type MDLL is composed of only main blocks of DLLs. As a result, it has simple structure with low power consumption. In addition, some circuit techniques are utilized to improve characteristics of each block. The detail circuit techniques employed in the design of the individual building blocks are presented as follows:

A. VCDL

Fig. 2 shows a Pseudo Differential Current-Starved Delay Element (PDCSDE) [12], used as basic delay cell in this work. As shown in Fig. 3, the delay of PDCSDE can change over a very broad range, but it is nonlinear with respect to the control voltage, so gain of delay line becomes larger as the operating frequency is reduced; gain of delay line is the slope of delay time curve versus control voltage. Therefore, the stability of the loop is undermined at lower frequencies. The other important problem with this structure is dead-zone. The dead-zone is a control region of the delay line, which cannot provide the delay [4]. The control voltage of delay cell is bounded by the supply voltage and the threshold voltage of the transistors.

In the proposed delay cell, shown in Fig. 4, nonlinear behavior over narrow band of control voltage is corrected by applying body bias technique [13] and variable bias voltage generators (Fig. 5). Transistor sizes for the delay cell and bias circuits are specified in tables I and II. The voltage conversion curves are shown in Figs. 6 and 7, which generate control voltages for starved transistors (MN1, MN2, MP1, MP2) from output voltage of loop filter (Vc). These circuits have two main functions: one is overcome the dead-zone issue, which allows the delay cell to operate at a lower control voltages and the other is to reduce the gain of the VCDL in low frequencies and improve the linearity.

Furthermore, to minimize the effect of the power supply and the substrate noise, two single ended current starved inverters are utilized in a differential structure. Each branch of delay cell is implemented as a two-stage inverter; delay cell value is adjusted by the current that flows through the first inverter. Pull-down gate/body control voltages (Vcn/VbodyN) and pull-up gate/body control voltages (Vcp/VbodyP) are changed symmetrically and continuously modulate the ON resistance of pull-down (MN1, MN2) and pull-up (MP1, MP2) transistors. These variable resistances control the current available to charge or discharge the load capacitance of the first inverter in the whole range of control voltage from 0.2V to 1V. As shown in Fig. 8, the slope of Modified Pseudo Differential Current-Starved Delay Element (MPDCSDE) is balanced and a good linearity in a wide dynamic range for the delay control signal is achieved. However, since overlap between two bias circuits is not supreme some nonlinearity exists near the 0.6V of control voltage.

Moreover, cross-coupled inverters are inserted at the output nodes to reduce the clock skew between the 0 and 180 clocks. The multiphase VCDL is composed of five delay cell units to generate the five multiphase output. In other words, each delay element produces on-chip five-phase clocks that are 72 degrees apart in one period.

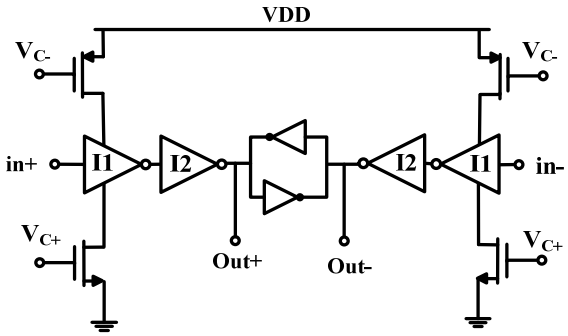


Fig. 2. Pseudo Differential Current-Starved Delay Element.

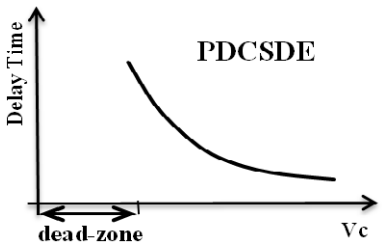


Fig. 3. Delay versus the control voltage.

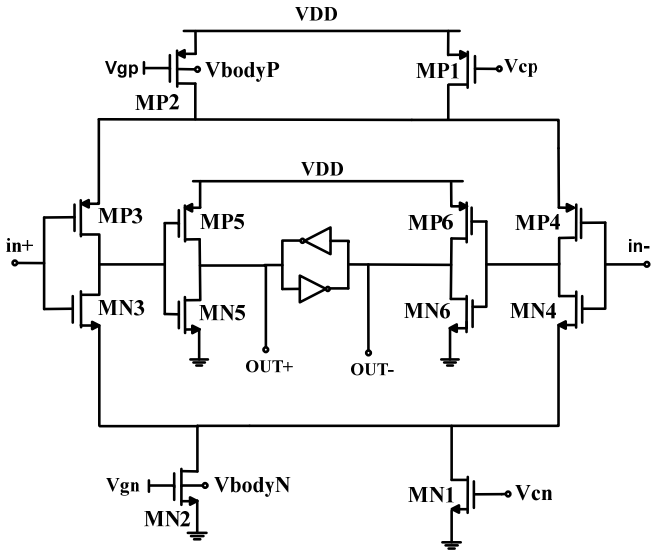


Fig. 4. Proposed delay cell.

TABLE I
DELAY CELL TRANSISTOR SIZES

MN1	MN2	MN3,4	MN5,6	MP1	MP2	MP3	MP4
0.54/0.18	0.36/0.27	2.7/0.18	0.45/0.18	1.8/0.19	0.54/0.18	2.7/0.18	0.9/0.18

TABLE II
BIAS CIRCUITS TRANSISTOR SIZES

MN1	MN2	MN3	MN4	MN5	MN6	MN7
1.35/0.18	0.27/0.9	0.72/0.18	2.25/0.18	0.45/0.81	0.27/0.72	0.27/0.45
MP1	MP2	MP3	MP4	MP5	MP6	MN8
0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.27	1.26/0.18	0.72/0.18	0.63/0.91

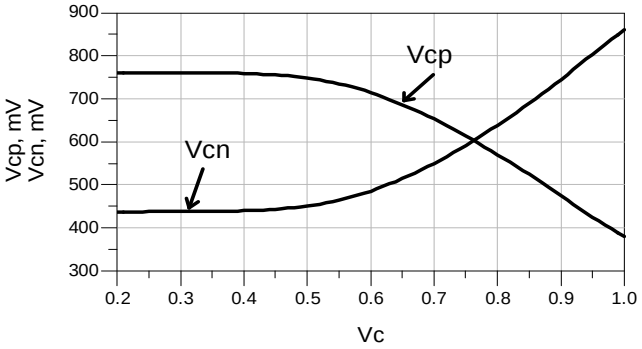


Fig. 6. DC curve of gate control voltage generator

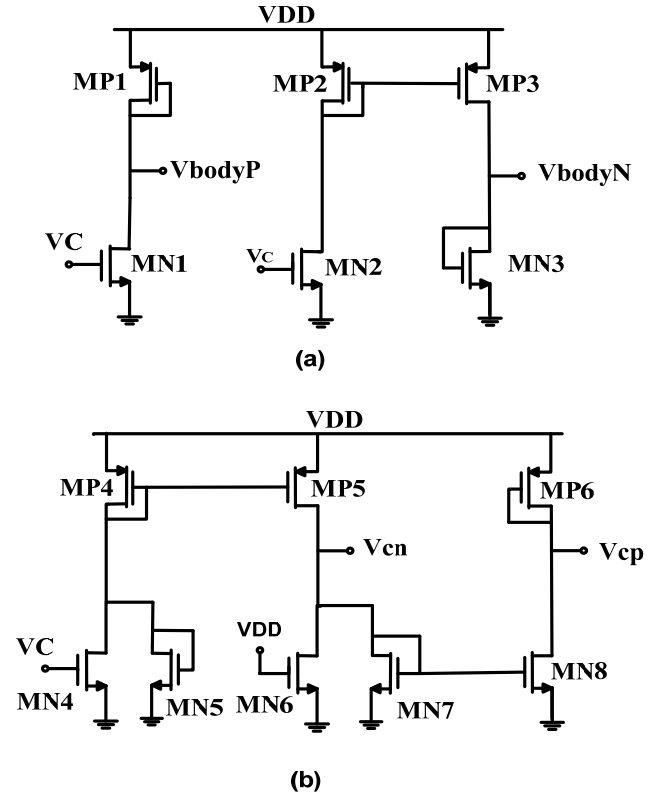


Fig. 5. Variable bias voltage generators (a) body control (b) gate control.

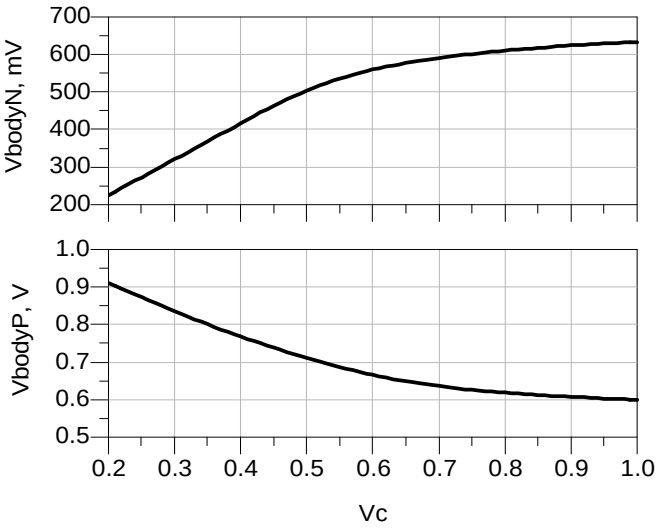


Fig. 7. DC curve of body control voltage generator.

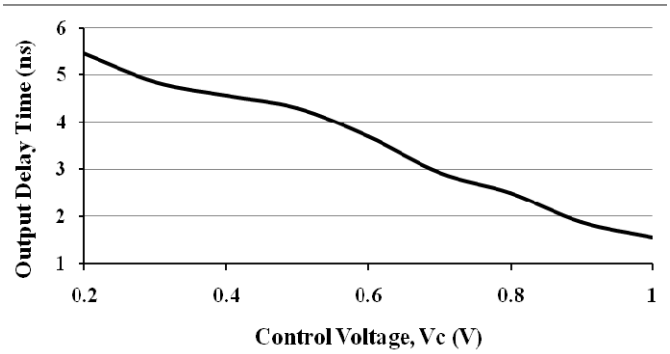


Fig. 8. Output delay versus control voltage.

B. Start Controlled PFD

To avoid the locking problem of analog DLL a start controlled circuit is utilized with PFD. The circuit has simple structure, short reset path, high operating frequency and low power consumption. Start controlled circuit has two functions. First, is to set the delay of VCDL to the minimum value. Second is to remain the feedback loop of DLL in sleep mode until start signal is not available. The adopted PFD comprise two NAND-Resettable dynamic DFFs. Since the DFFs are edge-trigger type, duty cycles of input signal and output signal are not required to be exactly 50% [4].

C. Self-Biased CP

In CMOS CPs usually PMOS switches and current mirrors are utilized for "UP" operation, and NMOS transistors for "DOWN" operation. Since the NMOS and PMOS transistors have non-identical characteristics, mismatch issue is inevitable in single-ended CPs [6].

This paper presents a control circuit to suppress the mismatch problem between Iup and Idn. The proposed bias circuit and self-biased charge pump are shown in Fig. 9 and 10. The main CP is composed of the transistors MN1, MN2, MP1, and MP2. The voltages VbiasP and VbiasN are the variable bias voltages of output current source and sink, respectively. The capacitor CL is used as the loop filter; MN1 and MP1 are utilized as the switches to control the functionality of charging or discharging the loop filter. Although "UP" and "DOWN" signals of PFD turn on each cycle, control circuit in the CP prevents that "UP" and "DOWN" switches to be activated simultaneously. the proposed charge pump behaviour can be described as follows:

While Vc is smaller than Vref, output signal of comparator (S) is high, so "UPB" and "DNB" signals direct to input of G1 and G2, respectively. Inversely, when Vc becomes larger than the Vref, "S" signal goes low and "UPBD" and "DNBD", which are delayed signals of "UPB" and "DNB" by "To", will be connected to G1 and G2, respectively.

At high frequencies where Vc is near the VDD and clock has narrow width, time difference between "UP" and "DOWN" signals is small. "UPB" and "DNB" signals are lead "UP" and "DOWN", respectively. This prevents detecting small phase errors signals and cause large static phase in high frequency. To solve this problem,"UP" and "DOWN" signal are delayed by "To" and applied to G1 and G2 earlier. In this way, small phase errors detection is possible. If "UPBD" and "DNBD" are applied at low frequencies too, "UP" and "DOWN" switches will be turn on for a short time in lock condition, so mismatch of NMOS and PMOS switches cause ripple on control voltage and increases output jitter. Thereby, in low frequencies UPB and DNB are applied to G1 and G2.

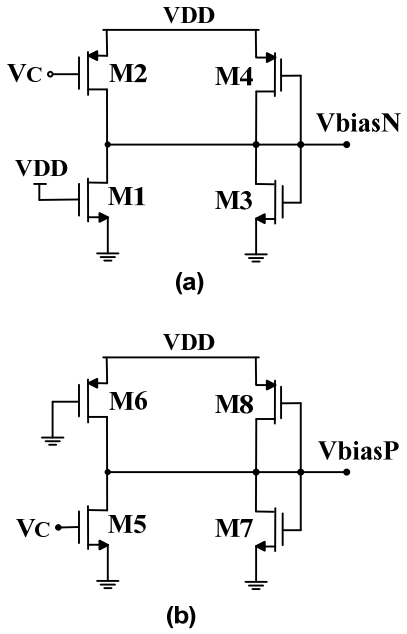


Fig. 9. Variable bias circuits for (a) current sink (b) current source.

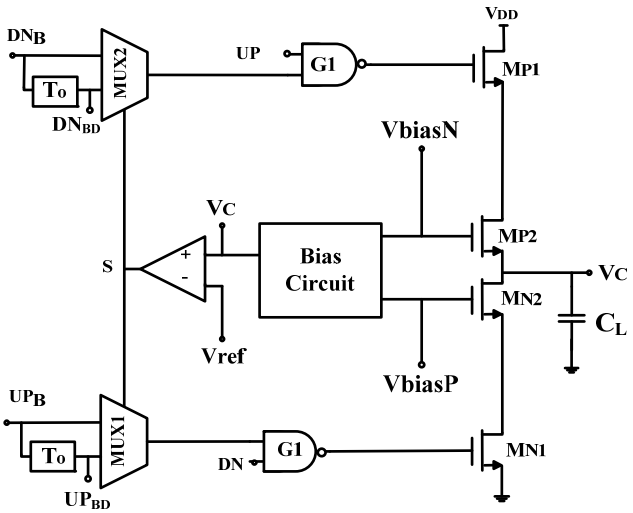


Fig. 10. Proposed charge pump.

TABLE III
BIAS CIRCUITS TRANSISTOR SIZES

M1	M2,3	M4	M5	M6	M7	M8
0.27/2.43	0.27/2.45	3.15/0.18	0.27/1.8	0.45/0.45	0.63/0.18	0.63/0.18

By using the proposed control circuit the need to precise current mirror is suppressed, so fixed bias voltages can be used to bias output transistors (MN2 and MP2) instead of current mirrors. But in this condition, because of transistor channel length modulation effect, Idn and Iup will drop once Vc approaches the ground potential (GND) or the supply voltage (VDD), respectively. As a result, the speed of the loop will be reduced at high and low frequencies. In this work, two bias circuits are used to compensate channel length modulation by changing gate voltages of MN2 and MP2 when Vc approaches GND and VDD, respectively. Fig. 9 (a) and (b) show the proposed bias circuits for Idn and Iup, respectively. Output bias voltages versus control voltage are shown in Fig. 11. The characteristic of current match between Iup and Idn with fixed bias voltage and proposed bias circuits are shown in Fig. 12 and 13, respectively. As can be shown in Fig. 13, in operation control voltage range (0.2 V to 1 V) both Iup and Idn are about 20 uA.

II. Simulation Result

The proposed circuit has been designed at transistor level and simulated by ADS, using 0.18um CMOS process. Locking process, consists of input and output signals, voltage of loop filter and charge pump output current and five multiphase outputs in lock condition at 185 MHz and 650 MHz have been shown in Figs. 14-17. Figs. 18 and 19 show static phase error and output rms jitter versus operation frequency. As can be seen, in low frequencies until "S" is high, jitter is good but the static phase error increases when frequency becomes bigger than 300 MHz, and in high frequencies until "S" is low static phase error is reasonable but jitter increases by decreasing frequency. Increasing jitter and static phase error is because of blind zone due to control circuit of CP.

As shown in Fig. 20 by increasing frequency, lock time of loop decreases from 50 ns to 14 ns until "S" is high and once "S" becomes low, lock time starts to increase from 15.5 ns to 32 ns. Fig. 21 shows dissipated power variation during the frequency range of DLL. Unlike the static phase error and jitter, power dissipation variation is independent of "S" situation, and increases proportional to frequency in whole of operation range. The maximum and minimum power dissipation at 650 MHz and 185 MHz are 1.1 mW and 0.37 mW, respectively.

In table IV performance of the proposed circuit is compared with some of previous reported designs. It must also be pointed out that the reported information for this work are extracted from the simulation results, whereas those of previously reported works are from the experimental results. So some problems such as parasitic elements, impedance mismatch and calibration errors have been ignored, which could influence the performance of proposed system for future fabrication and test setup.

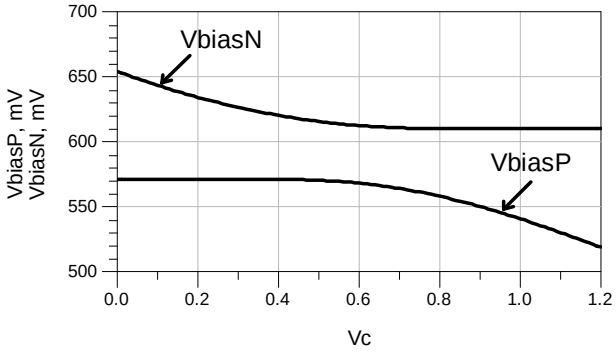


Fig. 11. DC curves of CP bias circuits.

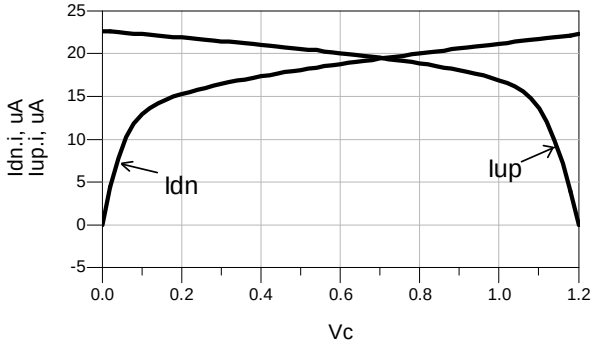


Fig.12. Iup and Idn versus Vc with fixed bias voltage.

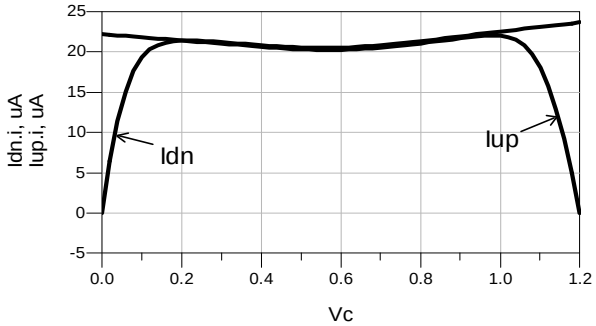


Fig. 13. Iup and Idn versus Vc after bias circuits applied.

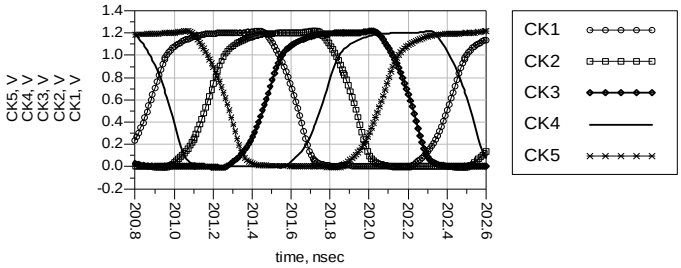


Fig. 14. Five multiphase outputs at 650 MHz.

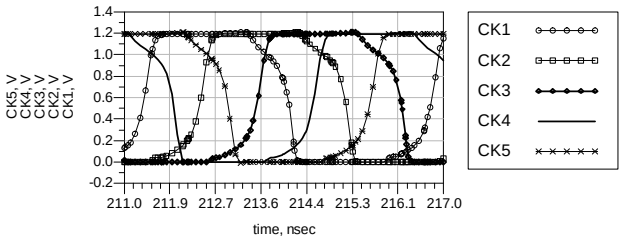
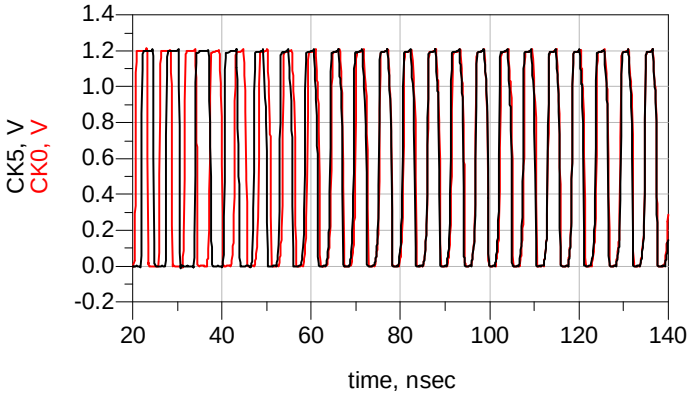
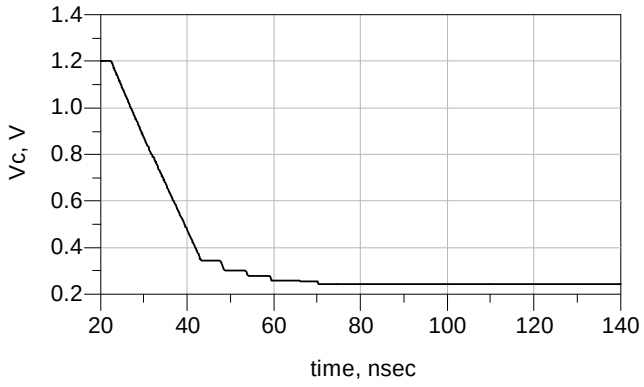


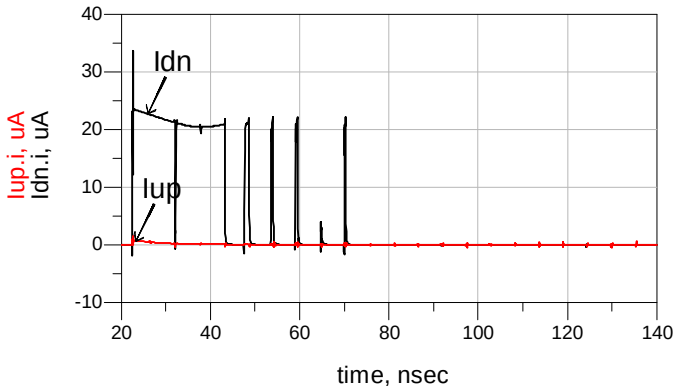
Fig. 16. Five multiphase outputs at 185 MHz.



(a)

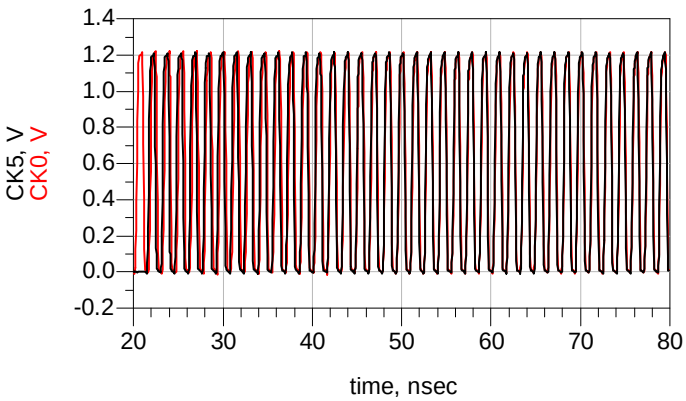


(b)

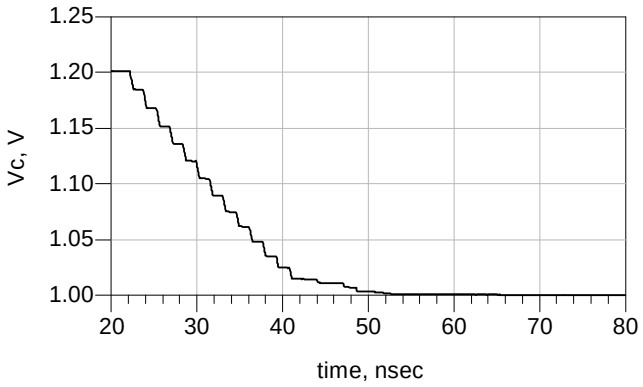


(c)

Fig. 15. DLL locking process at 185 MHz (a) CK0 and CK5 (b) Vc (c) Iup and Idn.



(a)



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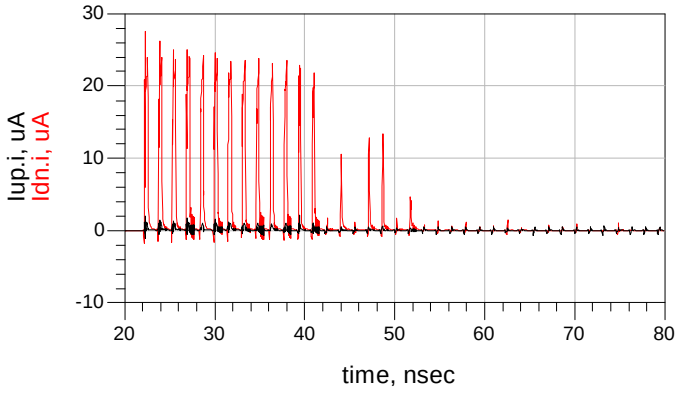

(c)

Fig. 17. DLL locking process at 650 MHz (a) CK0 and CK5 (b) Vc (c) Iup and Idn.

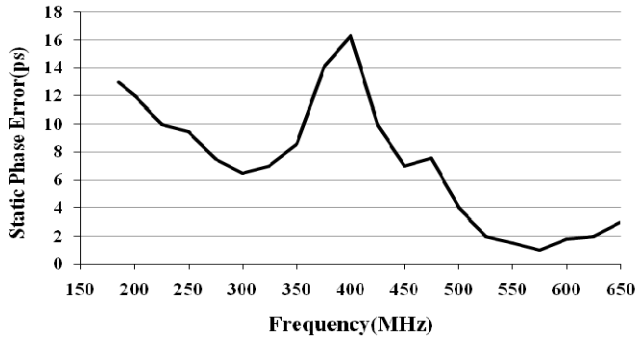

Fig. 18. Static phase error versus frequency

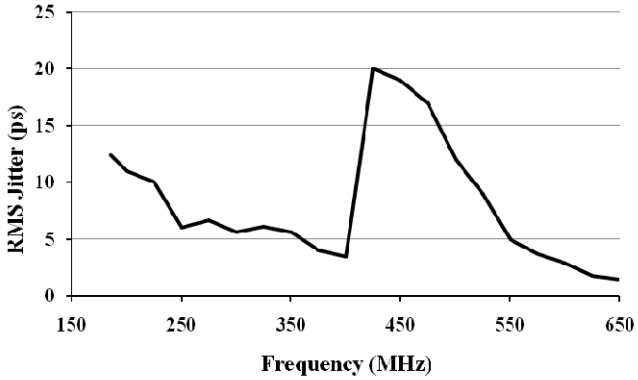

Fig. 19. RMS jitter versus frequency.

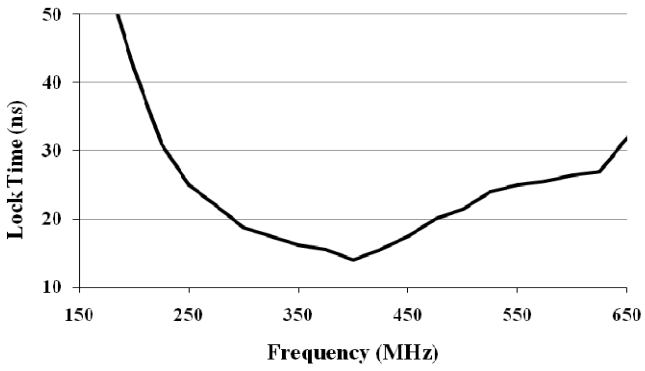

Fig. 20. Lock time versus frequency.

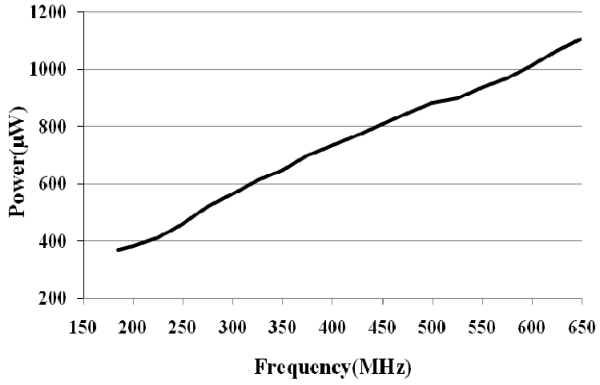

Fig. 21. Power dissipation versus frequency.

TABLE IV

PERFORMANCE COMPARISON

Performance parameter	**[15]**	**[13]**	**[3]**	**This work**
Process	0.25 μm	0.18 μm	0.18 μm	0.18 μm
Supply Voltage	2.5 V	0.6 V	1.8 V	1.2 V
Operation Range	32-320 MHz	85-550 MHz	150 - 400 MHz	185 - 650 MHz
Lock time	22 Cycles	N.A.	13 Cycles	21 Cycles
RMS jitter	4.44 ps @ 200 MHz	3.8 @ 550MHz	25 ps @ 400MHz	1.5 @ 650 MHz
Power dissipation	15 mW @ 320 MHz	4.2 @ 550MHz	N.A.	1.1 @ 650 MHz

III. CONCLUSION

This paper proposes a multiphase DLL with wide-range linear delay element and mismatch-free CP. By proper modification into pseudo differential current starved structure, a new delay line is proposed to use in designing the VCDL; by employing a forward bias voltage at the body terminal, good linearity with wide range operation is possible. In addition, this approach utilizes a new self-biased CP with a control circuit to eliminate mismatch problem in single-ended CPs. The circuit design and ADS simulation are carried out by TSMC 0.18 um CMOS process. Simulation results show that the frequency range of the suggested MDLL is from 185 to 650 MHz. Maximum, and minimum jitters are 20 and 1.5 ps respectively, and the maximum power dissipation at 650 MHz is 1.1 mW, so it is well suited for low-voltage and low-power applications.

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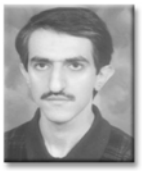

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